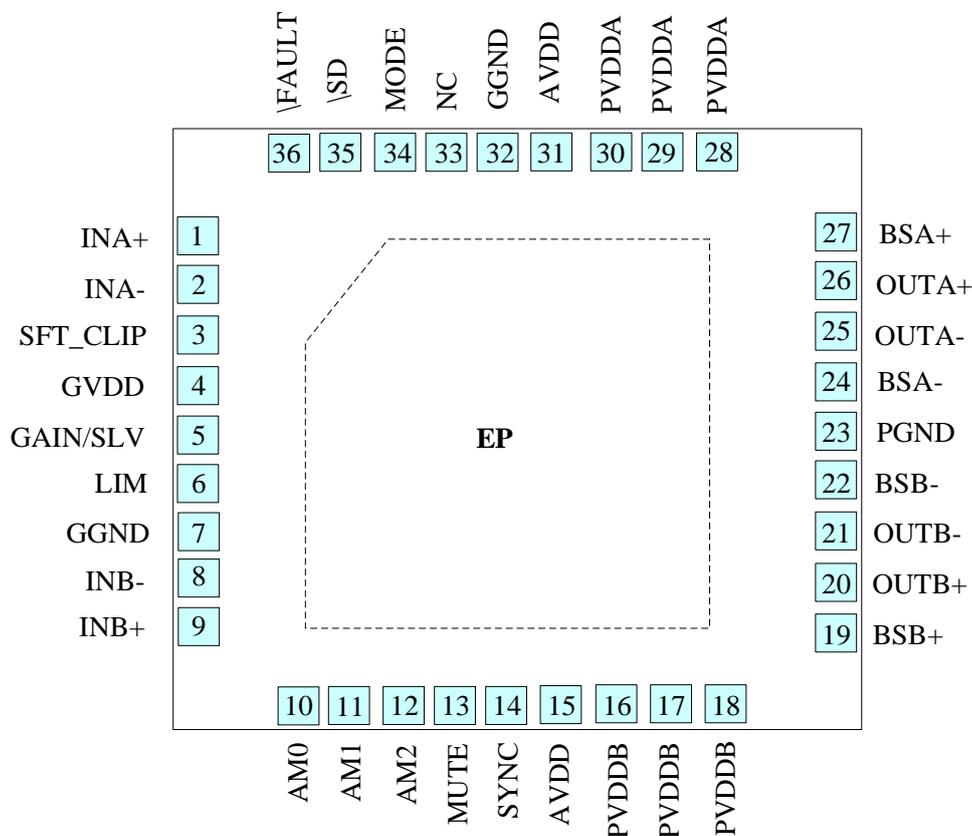


■ 引脚信息



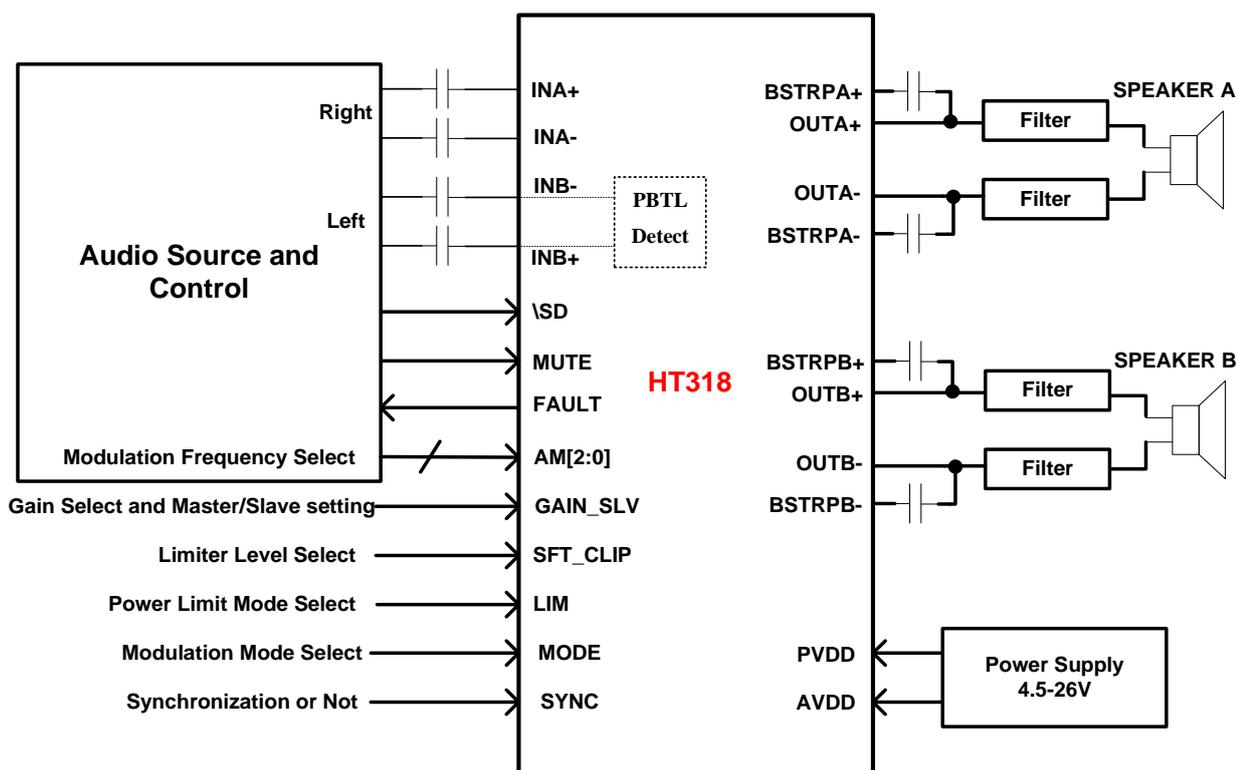
正视图

Pin No.	Name	I/O ²	Description
1	INA+	I	A通道正端音频输入
2	INA-	I	A通道负端音频输入
3	SFT_CLIP	I	设置输出最大限幅值
4	GVDD	O	内部整流输出, 接1uF电容到地
5	GAIN/SLV	I	增益设置, 或选择主从模式.
6	LIM	I	选择功率限制或AGC功能
7	GGND	G	栅极驱动地
8	INB-	I	B通道负端音频输入
9	INB+	I	B通道正端音频输入
10	AM0	I	D类调制频率选择
11	AM1	I	D类调制频率选择
12	AM2	I	D类调制频率选择
13	MUTE	I	静音设置, 引脚拉高是功放静音
14	SYNC	IO	多器件同步时, 时钟的输入输出脚, 作为输入还是输出取决于GAIN/SLV
15	AVDD	P	模拟电源输入端
16,17,18	PVDDB	P	B通道功率电源供电
19	BSB+	BST	Boot Strap端, 接220nF电容到OUTB+

² I: 输入; O: 输出; G: 地; P: 电源; BST: 自举

20	OUTB+	O	B通道输出正端
21	OUTB-	O	B通道输出负端
22	BSB-	BST	Boot Strap端，接220nF电容到OUTB-
23	PGND	G	功率地
24	BSA-	BST	Boot Strap端，接220nF电容到OUTA-
25	OUTA-	O	A通道输出负端
26	OUTA+	O	A通道输出正端
27	BSA+	BST	Boot Strap端，接220nF电容到OUTA+
28,29,30	PVDDA	P	A通道功率电源供电
31	AVDD	P	模拟电源供电
32	GGND	G	栅极驱动地
33	NC	-	内部无连接，可连接至地
34	MODE	I	D类调制模式选择，低时选择BD模式，高时选择1SPW模式
35	\SD	I	关断控制输入，低电平芯片处于低功耗状态；高电平芯片正常工作
36	\FAULT	O	功放错误检测输出，当芯片内部检测到错误，输出低电平
EP	PowerPad	G	芯片底部裸焊盘，请接电源地

■ 典型应用



75W PBTL/40W BTL Class D Stereo Amplifier with AM Avoidance

■ FEATURE

- Output Power (BTL)
2×40W ($V_{DD}=24V$, $R_L=8\Omega$, THD+N=1%)
2×30W ($V_{DD}=16V$, $R_L=4\Omega$, THD+N=10%)
- Output Power (PBTL)
75W ($V_{DD}=24V$, $R_L=4\Omega$, THD+N=10%)
- Single Wide Voltage Supply: 4.5V-26V
- Efficiency > 90%; BD and 1SPW Modulation
- Optional Power Limit Functions: AGC and Power Clipper (PCLP)
- Multiple Switching Frequency with AM Avoidance
- Master and Slave Synchronization
- Differential / Single-ended Analog Input, BTL or PBTL Output
- Integrated Self-protection Circuits Including Thermal Foldback (TFB) and Overvoltage, Undervoltage, Overtemperature, DC-detect, Overcurrent with Error Reporting
- LF and HF Package of QFN36L

■ APPLICATIONS

- Sound Bars · Wireless Speakers
- Consumer Audio Applications · TVs/Monitors

■ GENERAL DESCRIPTION

HT318 is a stereo efficient, Class-D audio amplifier for driving speakers up to 75W/4 Ω in mono PBTL. It can also deliver 2×30W/8 Ω power in stereo BTL.

HT318 features 2 different power limit functions. One is power clipper (PCLP), which can clip the output voltage under a preset level; another one is AGC which can limit the output music under a preset level without clipping.

Thermal Foldback (TFB) function is designed to protect HT318 from excessive die temperature in case of the device being operated beyond the recommended temperature or power, or with a weak thermal system, without shutting the device down.

Multiple switching Frequency is selectable for HT318 to avoid AM interferences. HT318 also can be worked in either master or slave, making it possible to synchronize multiple devices.

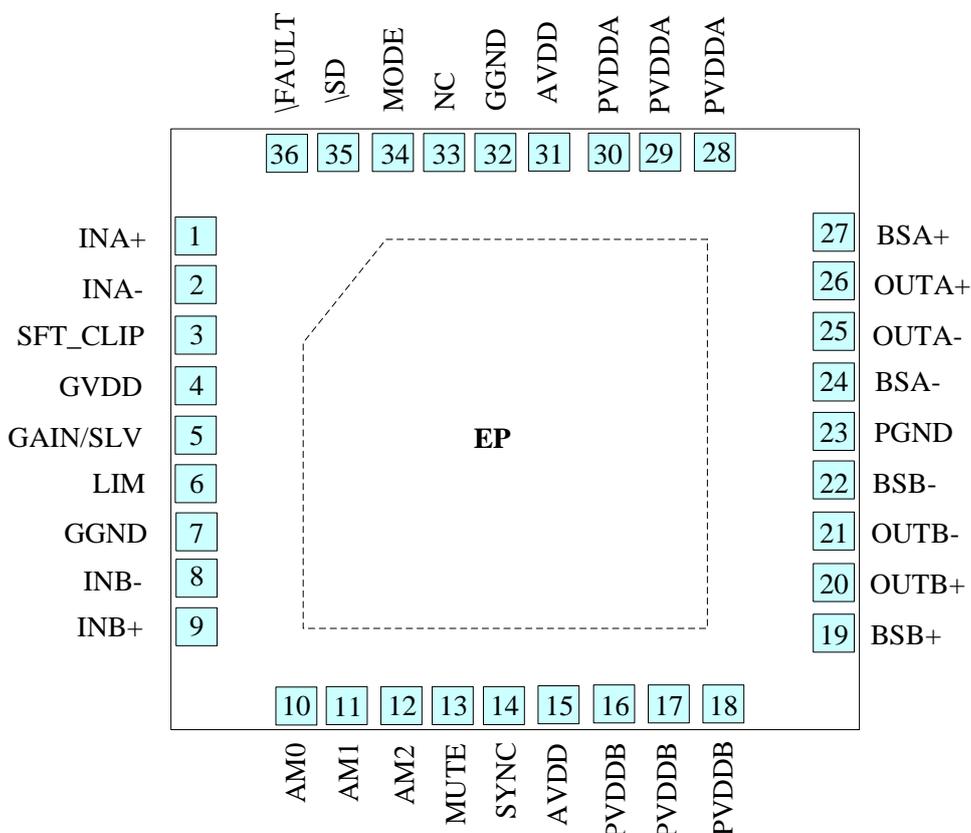
HT318 is fully protected against faults with Overvoltage, Undervoltage, Overtemperature, DC-detect, and Overcurrent protection. Faults can be reported to the processor to prevent devices from being damaged

■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	MOQ/Shipping Package
HT318SQER	QFN36L	HT318sq UVWXYZ ¹	-40°C ~ 85°C	Tape and Reel 2500PCS

¹ UVWXYZ is production tracking code

■ TERMINAL CONFIGURATION

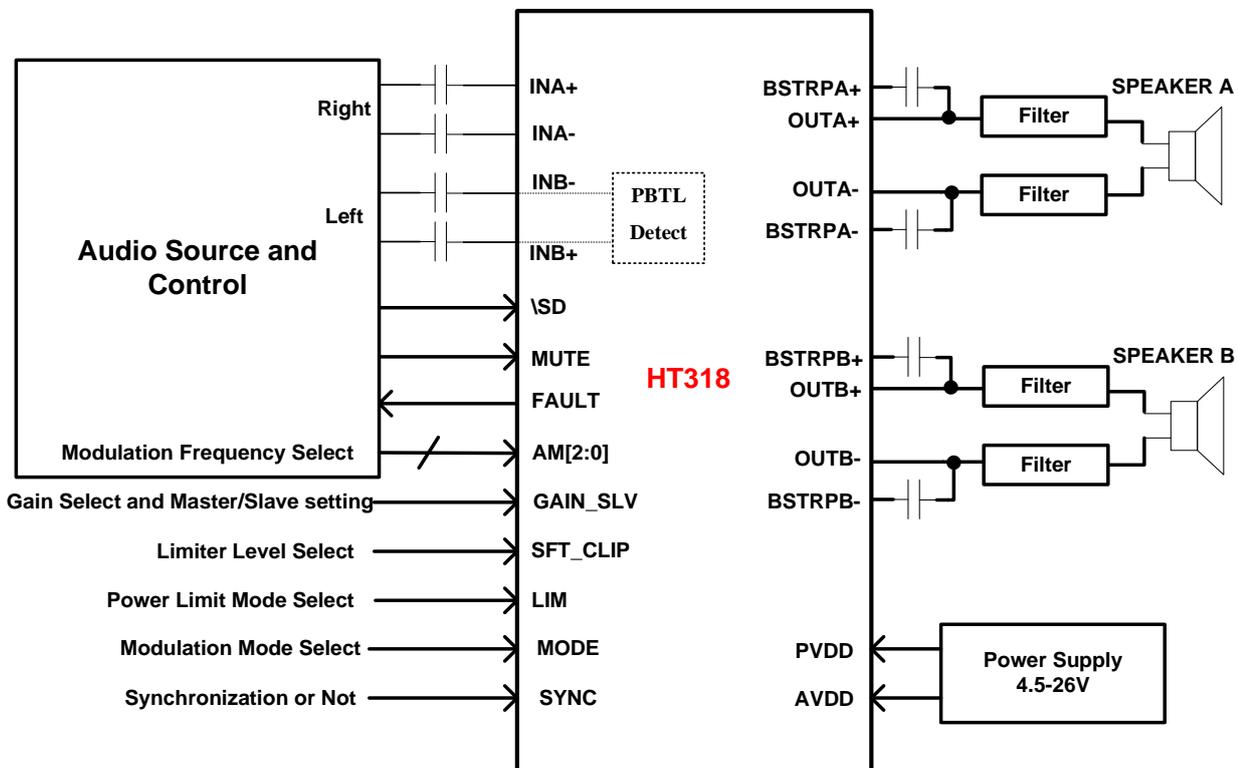


Top View

Pin No.	Name	I/O ¹	Description
1	INA+	I	Positive input terminal for A channel
2	INA-	I	Negative input terminal for A channel
3	SFT_CLIP	I	Sets the maximum output voltage before clipping (Limiter Level)
4	GVDD	O	Voltage regulator derived from PVDD supply, connect 1uF to GND (NOTE: This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
5	GAIN/SLV	I	Selects gain and selects between Master and Slave mode depending on pin voltage divider.
6	LIM	I	Selects the mode of Power Clipper or AGC
7	GGND	G	Ground for gate drive circuitry (this terminal should be connected to the system ground)
8	INB-	I	Negative input terminal for B channel
9	INB+	I	Positive input terminal for B channel
10	AM0	I	AM Avoidance Frequency Selection
11	AM1	I	AM Avoidance Frequency Selection
12	AM2	I	AM Avoidance Frequency Selection
13	MUTE	I	Mute control terminal, the amplifier is muted when it is pulled high
14	SYNC	IO	Clock input/output for synchronizing multiple class-D devices. Direction determined by GAIN/SLV terminal.
15	AVDD	P	Analog power supply

¹ I: Input; O: Output; G: Ground; P: Power; BST: Boot Strap

16,17,18	PVDDB	P	Power Supply for amplifier drivers of B channel
19	BSB+	BST	Connection point for the OUTB+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTB+
20	OUTB+	O	Positive pin for differential speaker amplifier output B
21	OUTB-	O	Negative pin for differential speaker amplifier output B
22	BSB-	BST	Connection point for the OUTB- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTB-
23	PGND	G	Power ground, make sure connect it to the system ground
24	BSA-	BST	Connection point for the OUTA- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTA-
25	OUTA-	O	Negative pin for differential speaker amplifier output A
26	OUTA+	O	Positive pin for differential speaker amplifier output A
27	BSA+	BST	Connection point for the OUTA+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTA
28,29,30	PVDDA	P	Power Supply for amplifier drivers of A channel
31	AVDD	P	Analog power supply
32	GGND	G	Ground for gate drive circuitry (this terminal should be connected to the system ground)
33	NC	-	Not connected inside the device (all "no connect" pins should be connected to ground for best thermal performance, however they can be used as routing channels if required.)
34	MODE	I	Mode selection logic input (LOW = BD mode, HIGH = 1 SPW mode). TTL logic levels with compliance to AVCC
35	\SD	I	Place the speaker amplifier in shutdown mode while pulled down.
36	\FAULT	O	Speaker amplifier fault terminal, which is pulled LOW when an internal fault occurs
EP	PowerPad	G	Connect to GND for best system performance.

TYPICAL APPLICATION


■ SPECIFICATIONS¹
● Absolute Maximum Ratings²

PARAMETER	Symbol	MIN	MAX	UNIT
Supply voltage range (PVDD, AVDD)	V _{DD}	-0.3	30	V
Input voltage range (INA+, INA-, INB+, INB-)	V _I	-0.3	5.8	V
Input voltage range (SFT_CLIP, GAIN/SLV, LIM, SYNC)	V _I	-0.3	GVDD	V
Input voltage range (AM0, AM1, AM2, MUTE, \SD, MODE)	V _I	-0.3	AVDD	V
Operating temperature range	T _A	-40	85	°C
Operating junction temperature range	T _J	-40	150	°C
Storage temperature range	T _{STG}	-50	150	°C

● Recommended Operating Conditions

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage range	V _{DD}	PVDD, AVDD	4.5		26	V
Operating temperature	T _a		-40	25	85	°C
High-level input voltage	V _{IH}	AMx, MUTE, \SD, SYNC, MODE	2			V
Low-level input voltage	V _{IL}	AMx, MUTE, \SD, SYNC, MODE			0.8	V
Low-level output voltage	V _{OL}	\FAULT			0.8	V
High-level input current	I _{IH}	AMx, MUTE, \SD, MODE (V _I = 2V, V _{DD} = 18V)			50	uA
Load impedance (BTL)	R _L	With output filter (10uH, 680nF)	3.2	4		Ω
Load impedance (PBTL)	R _L	With output filter (10uH, 1uF)	1.6	2		Ω

● DC Electrical Characteristics

Conditions: T_A = 25°C, V_{DD} = 4.5-26V, Load = 4ohm, unless otherwise specified.

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Class Output Offset Voltage	V _{OS}	V _I = 0V, Gain = 36dB		1.5		mV
Quiescent supply current	I _{DD}	V _{DD} = 12V, No Load		20		mA
		V _{DD} = 24V, No Load		32		mA
Quiescent supply current in Mute mode	I _{MUTE}	V _{DD} = 12V, With Load		13		mA
		V _{DD} = 24V, With Load		13		mA
Quiescent supply current in SD mode	I _{SD}	V _{DD} = 12V, With Load		50		uA
		V _{DD} = 24V, With Load		50		uA
System Gain in master mode (BTL or PBTL)	Gain	RP = open, RD = 5.6kΩ	35	36	37	dB
		RP = 100kΩ, RD = 20kΩ	31	32	33	dB
		RP = 100kΩ, RD = 39kΩ	25	26	27	dB
		RP = 75kΩ, RD = 47kΩ	19	20	21	dB
System Gain in slave mode (BTL or PBTL)	Gain	RP = 51k, RD = 51kΩ	35	36	37	dB
		RP = 47kΩ, RD = 75kΩ	31	32	33	dB
		RP = 39kΩ, RD = 100kΩ	25	26	27	dB
		RP = 16kΩ, RD = 100kΩ	19	20	21	dB
Turn-on time	t _{on}	Pull \SD high or power on		10		ms
Turn-off time	t _{off}	Pull \SD low		2		us
Gate drive supply	GVDD			5.5		V

¹ Depending on parts and PCB layout, characteristics may be changed.

² Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

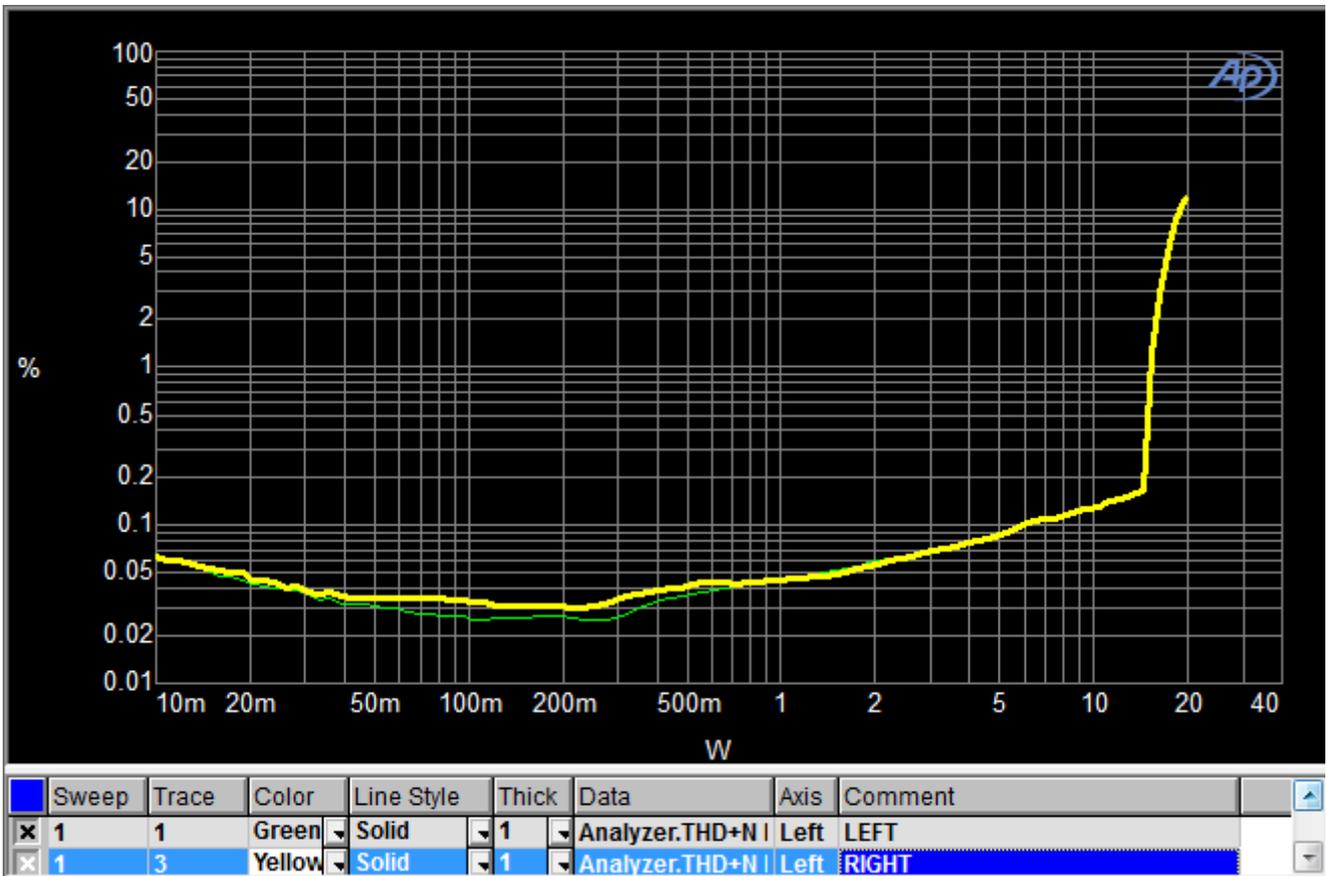
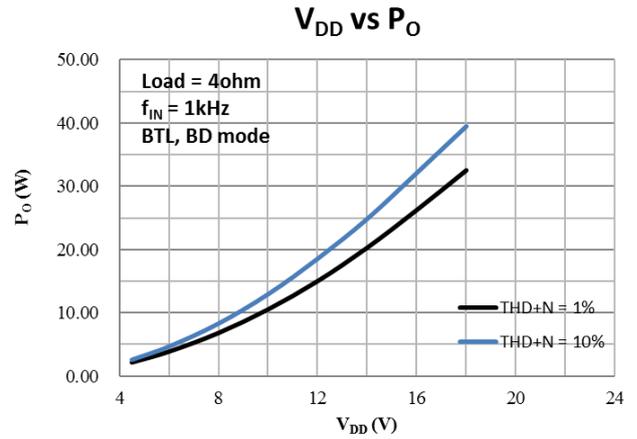
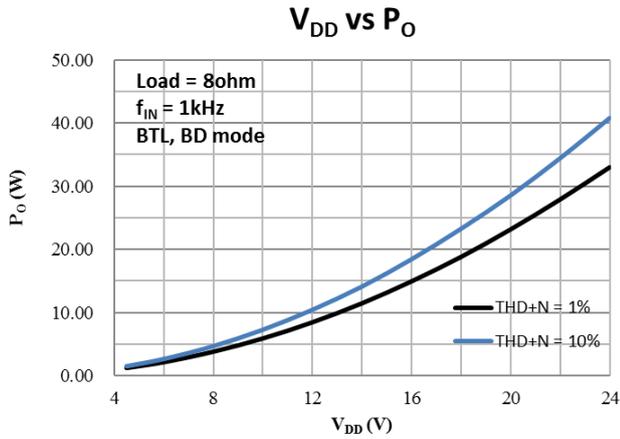
● **AC Electrical Characteristics**

Conditions: $T_A = 25^\circ\text{C}$, $V_{DD} = 4.5\text{-}26\text{V}$, Load = Filter + R_L , Filter = $10\mu\text{H} + 680\text{nF}$, $R_L = 4\Omega + 22\mu\text{H}$, $f_{IN} = 1\text{ kHz}$, Gain = 26dB, $C_{IN} = 1\mu\text{F}$, 20-20kHz, Power Limit off, BD mode, unless otherwise specified.

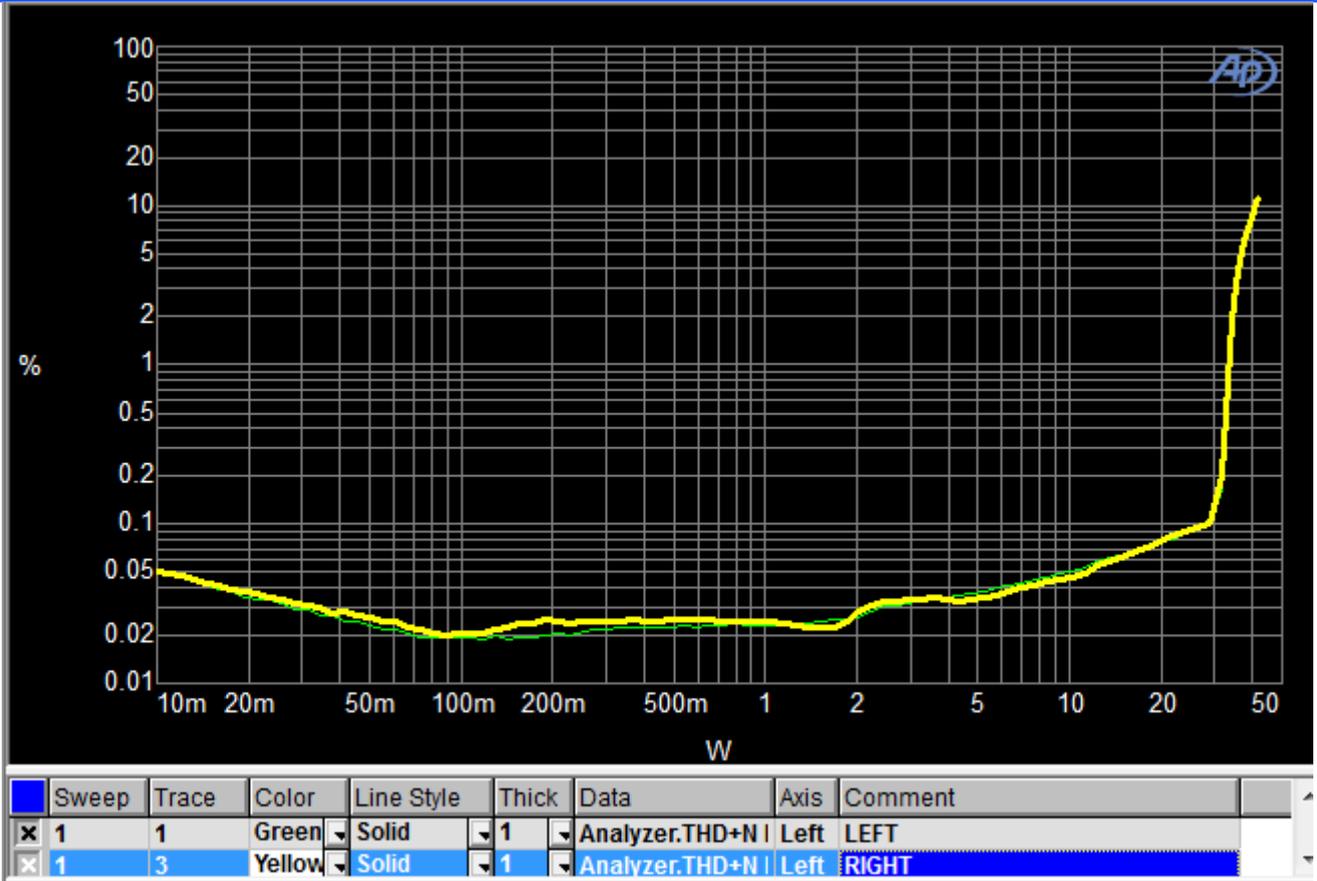
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Continuous output power	P_o	VDD = 12V, $R_L = 4\Omega + 22\mu\text{H}$, BTL	THD +N = 1%	14		W
			THD+N = 10%	17		W
		VDD = 12V, $R_L = 8\Omega + 33\mu\text{H}$, BTL	THD +N = 1%	8		W
			THD+N = 10%	10		W
		VDD = 16V, $R_L = 4\Omega + 22\mu\text{H}$, BTL	THD +N = 1%	26		W
			THD+N = 10%	30		W
		VDD = 16V, $R_L = 8\Omega + 33\mu\text{H}$, BTL	THD +N = 1%	15		W
			THD+N = 10%	18		W
		VDD = 20V, $R_L = 8\Omega + 33\mu\text{H}$, BTL	THD +N = 1%	23		W
			THD+N = 10%	28		W
		VDD = 24V, $R_L = 8\Omega + 33\mu\text{H}$, BTL	THD +N = 1%	33		W
			THD+N = 10%	40		W
		VDD = 16V, $R_L = 3\Omega + 22\mu\text{H}$, PBTL	THD +N = 1%	36		W
			THD+N = 10%	45		W
VDD = 16V, $R_L = 4\Omega + 22\mu\text{H}$, PBTL	THD +N = 1%	28		W		
	THD+N = 10%	35		W		
VDD = 20V, $R_L = 4\Omega + 22\mu\text{H}$, PBTL	THD +N = 1%	45		W		
	THD+N = 10%	55		W		
VDD = 24V, $R_L = 4\Omega + 22\mu\text{H}$, PBTL	THD +N = 1%	60		W		
	THD+N = 10%	75		W		
Total harmonic distortion + noise	THD+N	$P_o = 1\text{W}$, $V_{DD} = 18\text{V}$, $R_L = 8\Omega$		0.02		%
Efficiency	η	VDD = 12V, THD+N = 10%	$R_L = 4\Omega$, BTL	92		%
			$R_L = 8\Omega$, BTL	94		%
		VDD = 20V, THD+N = 10%	$R_L = 8\Omega$, BTL	94		%
		VDD = 16V, THD+N = 10%	$R_L = 4\Omega$, PBTL	95		%
Cross Talk	CT	$V_o = 1\text{V}_{rms}$, Gain = 20dB		-95		dB
Output integrated noise	V_N	A-weighted, Gain = 20 dB		100		μV
Signal-to-noise ratio	SNR	A-weighted, Gain = 20 dB, $P_o = 1\text{W}$		85		dB
Power supply rejection ratio	PSRR	200mVpp 1kHz, Input grounded		-75		dB
Oscillator frequency	f_{osc}	AM2=0, AM1 = 0, AM0 = 0		400		kHz
		AM2=0, AM1 = 0, AM0 = 1		500		kHz
		AM2=0, AM1 = 1, AM0 = 0		600		kHz
		AM2=0, AM1 = 1, AM0 = 1				Reserved
		AM2=1, AM1 = 0, AM0 = 0				
		AM2=1, AM1 = 0, AM0 = 1				
		AM2=1, AM1 = 1, AM0 = 0				
AM2=1, AM1 = 1, AM0 = 1						
Over temperature protection trigger point	OTP			160		$^\circ\text{C}$
Thermal holdback trigger point	TFB			150		$^\circ\text{C}$
Over current trip point	OCP			7.5		A

■ TYPICAL OPERATING CHARACTERISTICS

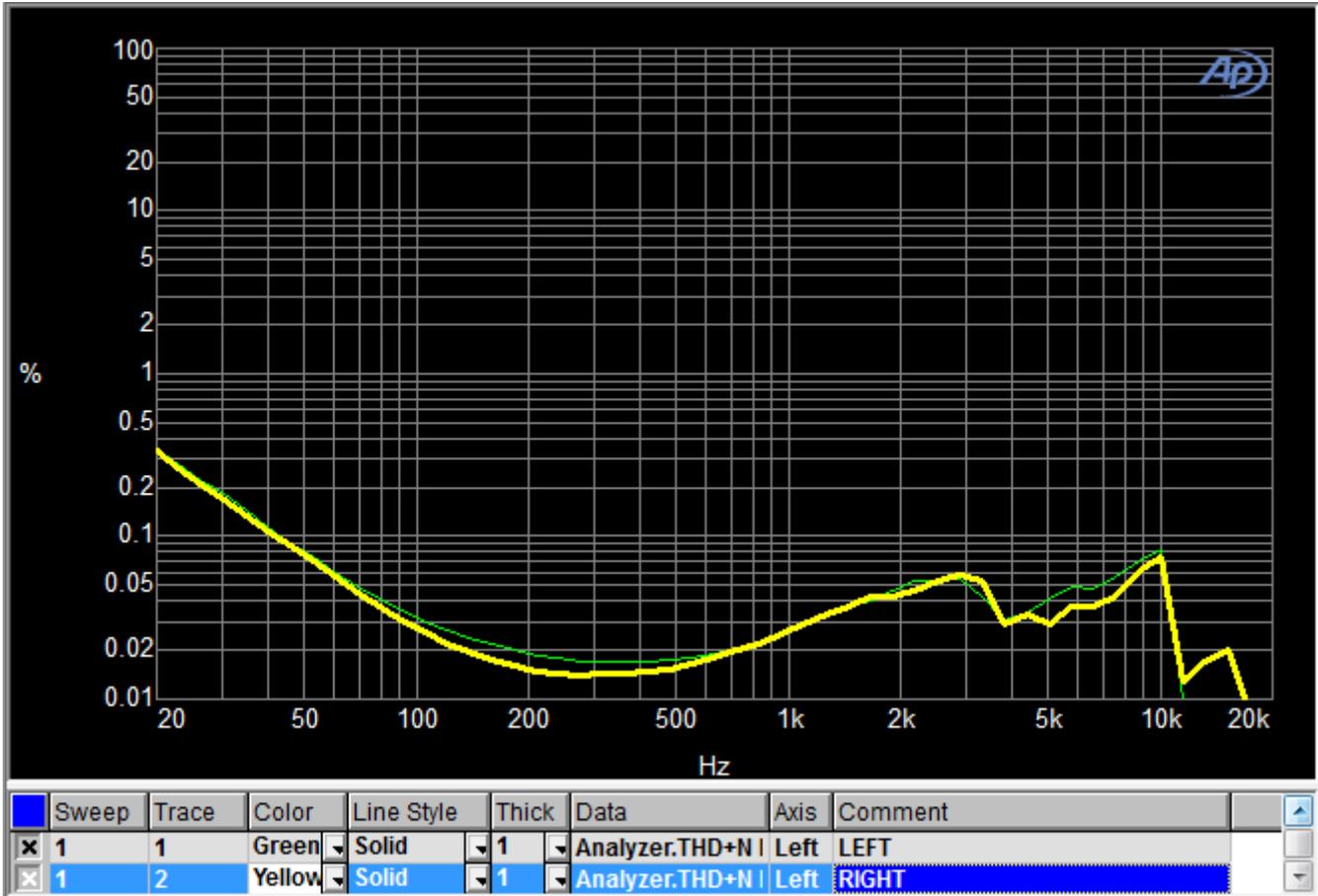
$T_A = 25^\circ\text{C}$, **BTL mode**, $AM1 = AM2 = L$, $MODE = L$, $f_{IN} = 1\text{ kHz}$, unless otherwise noted. Output filter is used as $10\ \mu\text{H}$ and $0.68\ \mu\text{F}$, unless otherwise noted.



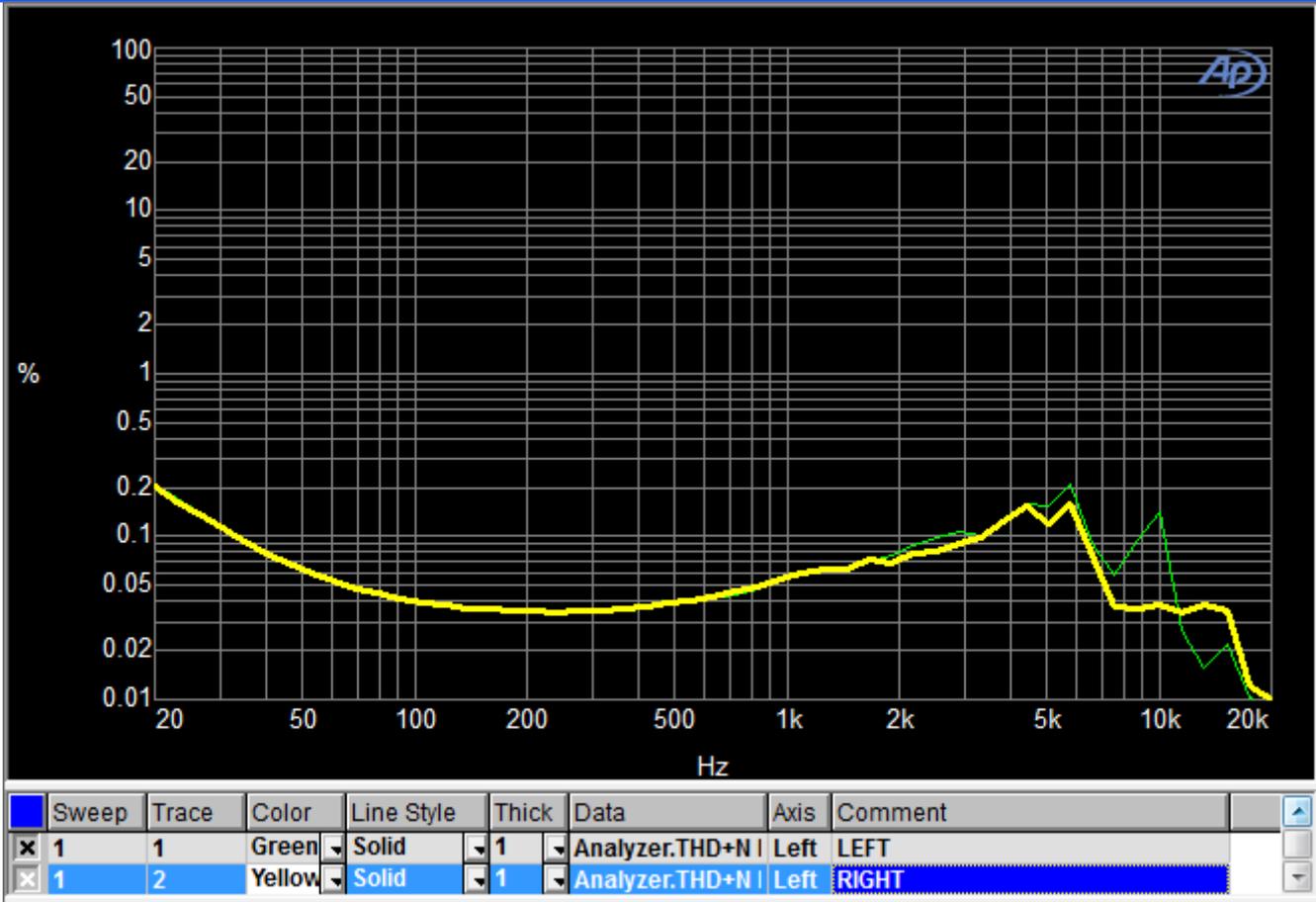
Po vs THD+N ($V_{DD} = 12\text{V}$, Load = 4ohm)



Po vs THD+N (VDD = 24V, Load = 8ohm)



f_{IN} vs THD+N (VDD = 24V, Load = 8ohm, Po = 1W)



f_{in} vs THD+N (VDD = 12V, Load = 4ohm, Po = 1W)

■ APPLICATION INFORMATION

1. Power Supply

The power supply for the HT318 only require one voltage from 4.5V to 26V, which supplies the analog circuitry (AVDD) and the power stage (PVDD)

The AVDD supply feeds internal LDO including GVDD. This LDO output is connected to external pins for filtering purposes, but should not be connected to external circuits. The filtering capacitor for GVDD is recommended to be 1uF. A filtering capacitor of 1uF for AVDD is also needed.

The PVDD (pin16, 17, 18) feeds the power stage of B channel and the PVDD (pin28, 29, 30) feeds the power stage of A channel. Filtering capacitors of 100nF//1uF//220uF for PVDD of each channel should be placed close to the PVDD pin.

2. Class D Modulation (MODE pin)

HT318 can run in either BD modulation or 1SPW modulation, which is determined by MODE pin.

2.1 BD modulation

BD modulation is selected once MODE pin is pulled low.

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage.

The OUT+ and OUT- are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUT+ is greater than 50% and OUT- is less than 50% for positive output voltages.

The duty cycle of OUT+ is less than 50% and OUT- is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I²R losses in the load.

2.2 1SPW modulation

1SPW modulation is selected once MODE pin is pulled high.

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection.

In 1SPW mode the outputs operate at ~15% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle.

Efficiency is improved in this mode due to the reduction of switching losses. The THD penalty in 1SPW mode is minimized by the high-performance feedback loop. The resulting audio signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.

3. Power Limit Function

There are two different power limit functions for HT318, one is Automatic Gain Control (AGC), the other is Power Clipper (PCLP). The function can be selected by setting the LIM pin.

3.1 Power Limit Mode (LIM pin)

The LIM pin configuration is shown as Figure 1 and Table. 1.

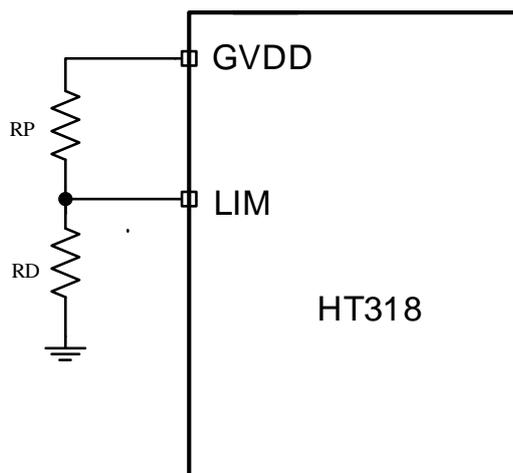


Figure 1 LIM Terminal Configuration

Table. 1 LIM Terminal Settings

Voltage of LIM Terminal	Power Limit Mode	Attack Time T_A (us/dB)	Release Time T_R (ms/dB)
GVDD	AGC FAST	80	400
2/3 GVDD	AGC MEDIUM	160	800
1/3 GVDD	AGC SLOW	320	1600
GND	PCLP		/

If the AGC function is selected, the output music can be limited below the preset Limiter Level (see pin SFT_CLIP). If the output audio signal exceeds the Limiter Level, HT318 decreases amplifier gain by the rate of attack time by 0.25dB per step (step pace). HT318 increases the gain by the rate release time by 0.25dB/step (step pace) once the output audio is below the limiter level. Figure 2 shows this relationship.

The AGC function don't clip the output wave while limiting the output power. It can remove the output clipping noise and protect the speakers caused by a reduction of power supply voltage or a sudden large volume of input music.

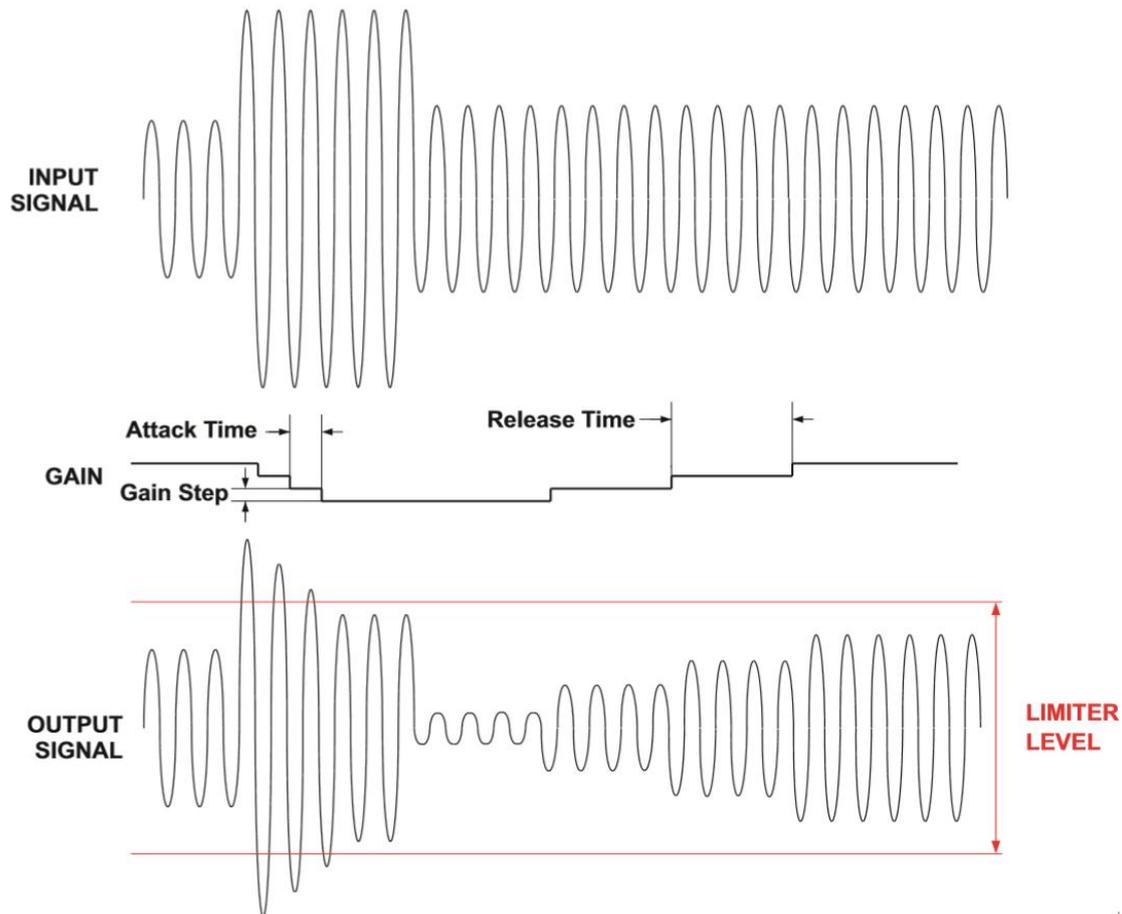


Figure 2 AGC Function Description

The HT318 also has a power clipper function (PLCP) that can be used to clip the output voltage level below the supply rail. The PLCP function can be selected by pulling LIM pin down into system ground, shown as Table. 1 LIM Terminal Settings.

When PLCP function is active, the amplifier operates as if it was powered by a lower supply voltage, and thereby enters into clipping sooner than if the circuit was not active. The result is clipping behavior very similar to that of clipping at the PVDD rail, in contrast to the digital clipper behavior which occurs in the oversampled domain of the digital path. The point at which clipping begins is called the Limiter Level (see pin SFT_CLIP).

To move the output stage into clipping, the PCLP function limits the duty cycle of the output PWM pulses to a fixed maximum value. After filtering this limit applied to the duty cycle resembles a clipping event at a voltage below that of the PVDD level.

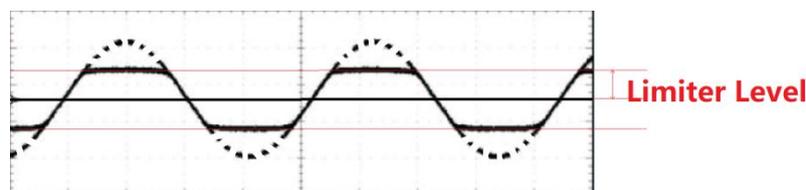


Figure 3 PCLP Function Description

3.2 Limiter Level Configuration (SFT_CLIP pin)

The Limiter Level is controlled by a resistor divider from GVDD (around 5.5V) to ground, which sets the voltage at the SFT_CLIP pin (V_{SFT_CLIP}). The Limiter Level is approximately 4 times the voltage at the SFT_CLIP pin, noted as V_{SFT_CLIP} .

$$\text{Limiter Level} \approx 4 \times V_{SFT_CLIP}$$

The precision of the threshold at which clipping occurs is dependent upon the voltage level at the SFT_CLIP pin. Because of this, increasing the precision of the resistors used to create the voltage divider, or using an external reference will increase the precision of the point at which the device enters into clipping. To ensure stability, and soften the edges of the clipping event, a capacitor should be connected from pin SFT_CLIP to ground.

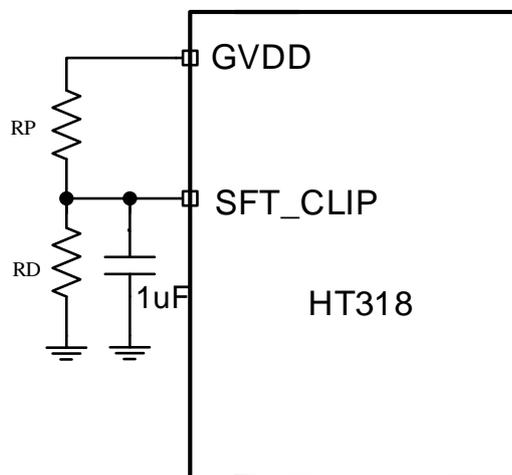


Figure 4 SFT_CLIP Terminal Configuration

If LIM pin is connected to GND, and SFT_CLIP pin is directly connected to GVDD, neither function of AGC nor PCLP is selected.

4. AM Avoidance EMI Reduction (AM0, AM1 pin)

To reduce interference in the AM radio band, the HT318 has the ability to change the switching frequency via AM1 AM0 pins. The recommended frequencies are listed in Table. 2.

Table. 2 Switching Frequency Settings

Switching Frequency (kHz)	AM2:AM1:AM0
400	000 (default)
500	001
600	010
Reserved	011
	100
	101
	110
	111

5. Gain Setting and Master and Slave (GAIN/SLV pin)

In order to select the amplifier gain setting, the designer must determine the maximum power target and the speaker impedance. Once these parameters have been determined, calculate the required output voltage swing which delivers the maximum output power.

Choose the lowest analog gain setting that corresponds to produce an output voltage swing greater than the required output swing for maximum power. The analog gain can be set by selecting the voltage divider resistors (RP and RD) on the Gain pin.

Master or Slave mode is also controlled by this pin. Notice that a gain or mode changing by this pin will be not effective when the amplifier is working.

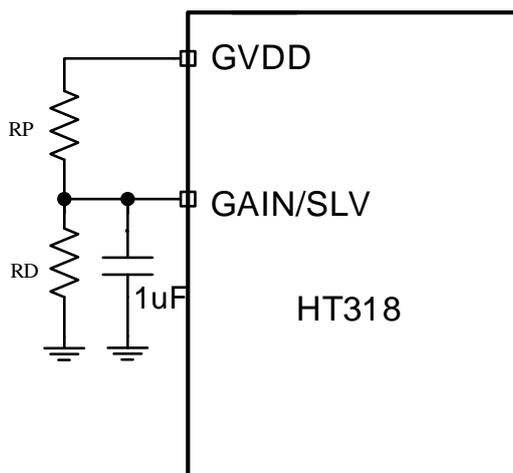


Figure 5 GAIN/SLV Terminal Configuration

Table. 3 GAIN/SLV Terminal Settings

RP (Ω)	RD (Ω)	Gain (dB)	Master or Slave Mode
NC	5.6k	36	Master
100k	20k	32	Master
100k	39k	26	Master
75k	47k	20	Master
51k	51k	36	Slave
47k	75k	32	Slave
39k	100k	26	Slave
16k	100k	20	Slave

6. Amplifier Input and Output

6.1 Amplifier Input Configuration

HT318 is an amplifier with analog input (single-ended or differential). For a differential operation, input signals into IN+ and IN- pins via DC-cut capacitors (C_{IN}). The high pass cut-off frequency of input signal can be calculated by

$$f_c = \frac{1}{2\pi R_{IN} C_{IN}}$$

For a single-ended operation, input signals to IN+ pin via a DC-cut capacitor (C_{IN}). IN- pin should be connected to ground via a DC-cut capacitor (with the same value of C_{IN}).

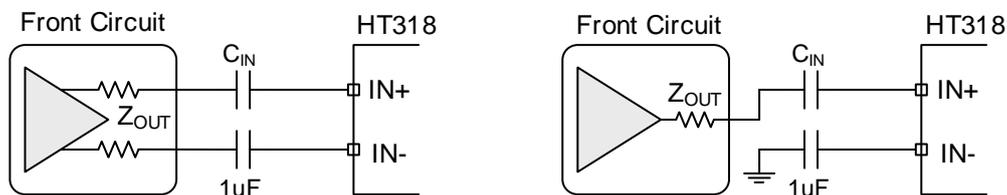


Figure 6 (1) Differential Input;

(2) Single-ended Input

The input impedance changes with the gain setting from 9kohm to 60kohm as Table 4. If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. Table 4 lists the recommended ac-couplings capacitors for each gain step. If a -3 dB is accepted at 20 Hz 10 times lower capacitors can be used – for example, a 1μF can be used.

Table. 4 R_{IN} vs GAIN vs C_{IN}

Gain (dB)	R_{IN} (k Ω)	C_{IN} (μ F)	f_c (Hz)
36	9	10	1.8
32	15	5.6	1.9
26	30	3.3	1.6
20	60	1.5	1.8

6.2 Amplifier Output Configuration

The HT318 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 20 cm and high power. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the class-D amplifier. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz. Also, the filter capacitor can be increased if necessary, with some impact on efficiency.

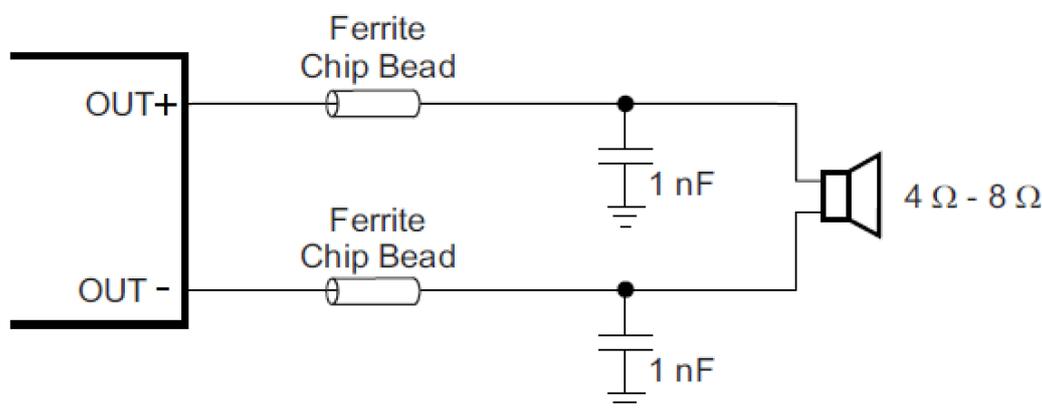


Figure 7 Output Filters with Ferrite Beads

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

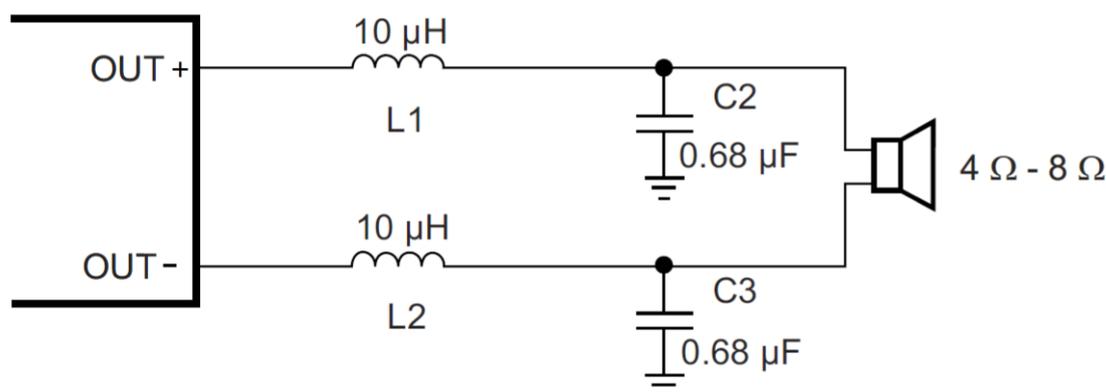


Figure 8 Output Filters with LC

6.3 PBTL Mode Configuration

The HT318 can be configured to drive a single speaker with the two output channels connected in parallel. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode. This mode of operation effectively reduces the output impedance of the amplifier in half, which in turn reduces the power dissipated in the device due to conduction losses through the output FETs. Additionally, since the output channels are working in parallel, it also doubles the amount of

current the speaker amplifier can source before hitting the over-current error threshold.

To place the HT318 into PBTL Mode, the PBTL pin should be pulled HIGH (that is, connected to the DVDD supply through a pull-up resistor). If the device is to operate in BTL mode instead, the PBTL pin should be pulled LOW, that is connected to the system supply ground. When operated in PBTL mode, the output pins should be connected as shown in the Typical Application Circuit Diagrams.

In PBTL mode, the amplifier selects its source signal from the A channel of the stereo signal.

7. Startup, Shutdown and Mute Operation

The HT318 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for power conservation. The \backslash SD input terminal should be held high during normal operation when the amplifier is in use. Pulling \backslash SD low will put the outputs to mute and the amplifier to enter a low-current state. It is not recommended to leave \backslash SD unconnected, because amplifier operation would be unpredictable.

For a better power on and power-off pop performance, place the amplifier in the shutdown mode prior to delivering or removing the power supply.

The HT318 also has a mute function in which the differential output is grounded through resistivity. The MUTE terminal should be held low in normal operation. Pulling MUTE high will put HT318 into MUTE mode. The noise of placing the amplifier in and out of mute mode will be lower than shutdown mode.

8. Other Functions and Terminals

8.1 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the SFT_CLIP, LIM and GAIN voltage dividers. Decouple GVDD with a X5R ceramic 1 μ F capacitor to GND. The GVDD supply is not intended to be used for external supply. It is recommended to limit the current consumption by using resistor voltage dividers for GAIN and SFT_CLIP of 100 k Ω or more.

8.2 BSx和BSBx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

9. Protection Functions

The HT318 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage.

9.1 Over Temperature Protection (OTP)

This is the function to establish the over temperature protection mode when detecting excessive high temperature of HT318. When the on-die temperature of HT318 is higher than TOP, the OTP mode is activated, the differential output pin becomes weak low state (a state grounded though resistivity).

9.2 Foldback (TFB) Function

The HT318 Thermal Foldback, TFB, is designed to protect the HT318 from excessive die temperature in case of the device being operated beyond the recommended temperature or power limit, or with a weaker thermal system than recommended, without shutting the device down.

The TFB works by reducing the on-die power dissipation by reducing the HT318 system gain by the rate of attack time (default value 1200ms/dB) by 0.25dB per step (step pace) if the TFB trig point is exceeded. Once the die temperature drops below the TFB trig point, the HT318 gain is increased by a single or by the rate of release time (default value 2400ms/dB) by 0.25dB per step (step pace) until the TFB trig point, or a maximum attenuation is reached, and the system gain will be decreased again, or the system gain is at its nominal gain level. The procedure shows as follows.

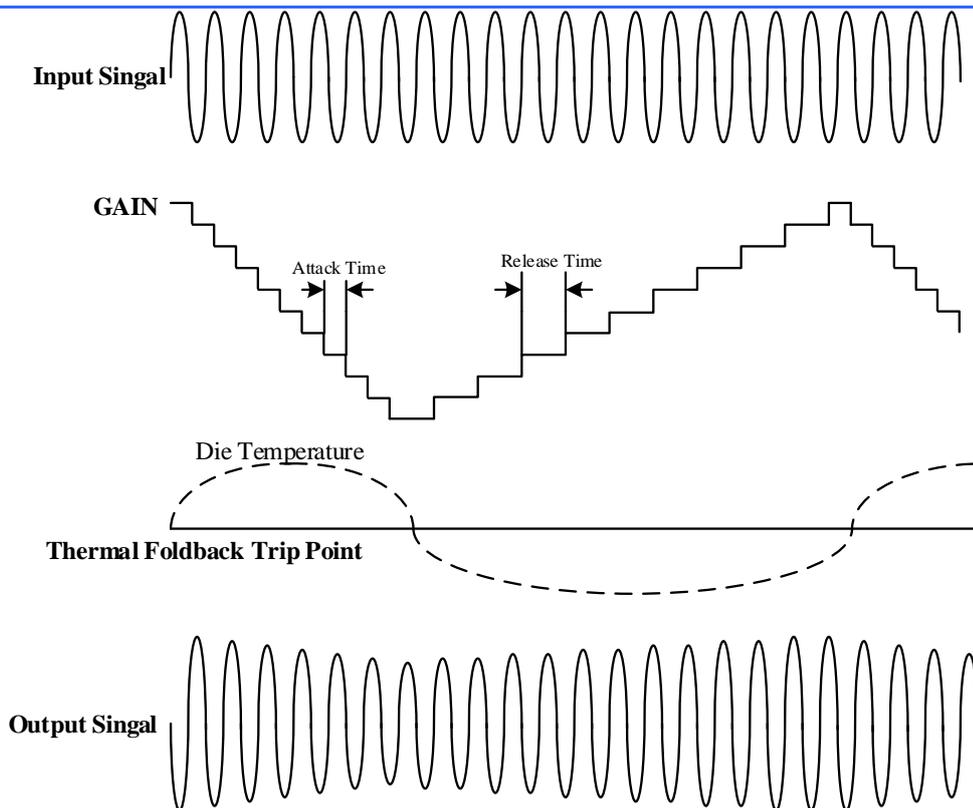


Figure 9 TFB Operation

9.3 DC Detect Protection (DCP)

The HT318 has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error.

A DCE event occurs when the output differential duty-cycle of either channel exceeds 60% for more than 420 msec at the same polarity. The table below shows some examples of the typical DCE Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2 Hz.

The minimum output offset voltages required to trigger the DC detect are listed in Table. 2. The outputs must remain at or above the voltage listed in the table for more than 420 msec to trigger the DC detect.

Table. 5 DC Detect Threshold

PVDD (V)	V _{os} (V)
4.5	0.96
6	1.3
12	2.6
18	3.9

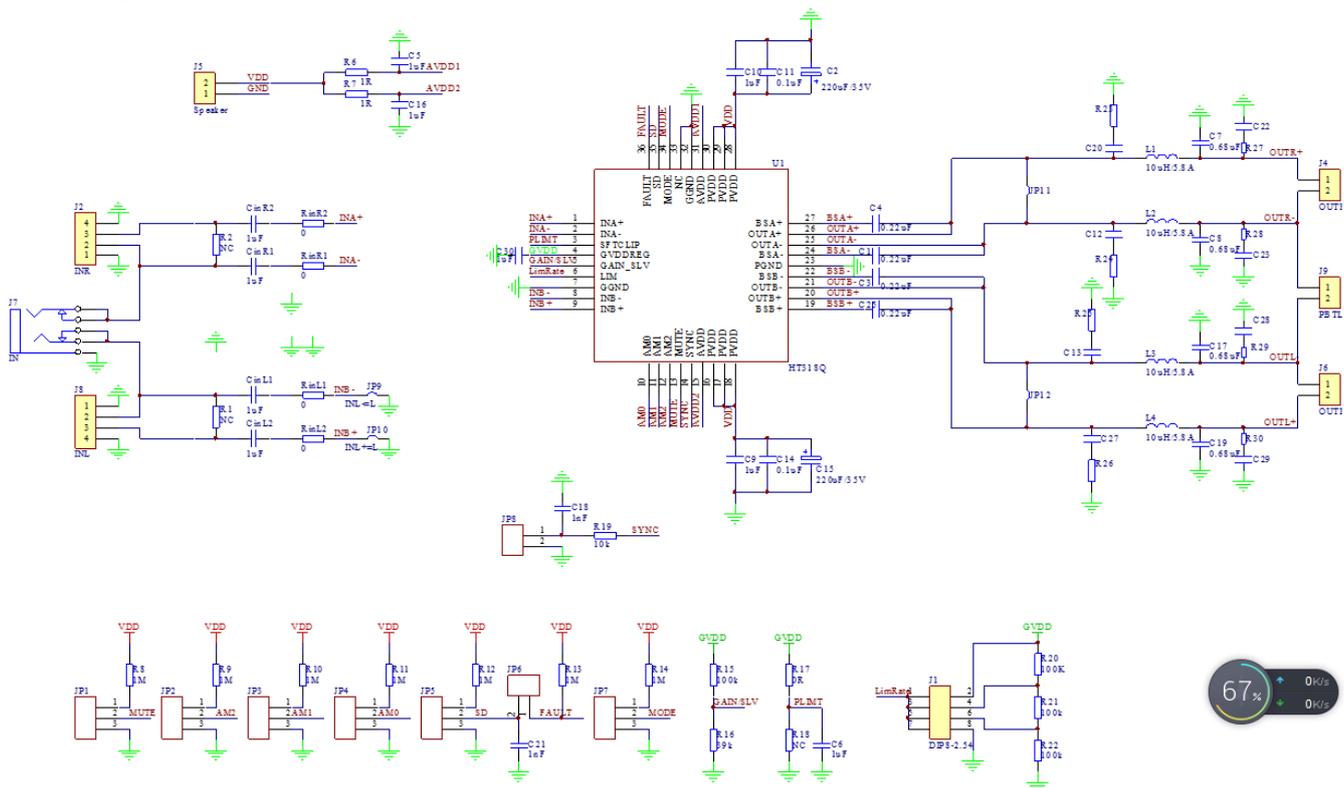
9.4 Short-Circuit Protection (OCP)

The HT318 has protection from over current conditions caused by a short circuit on the output stage. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged.

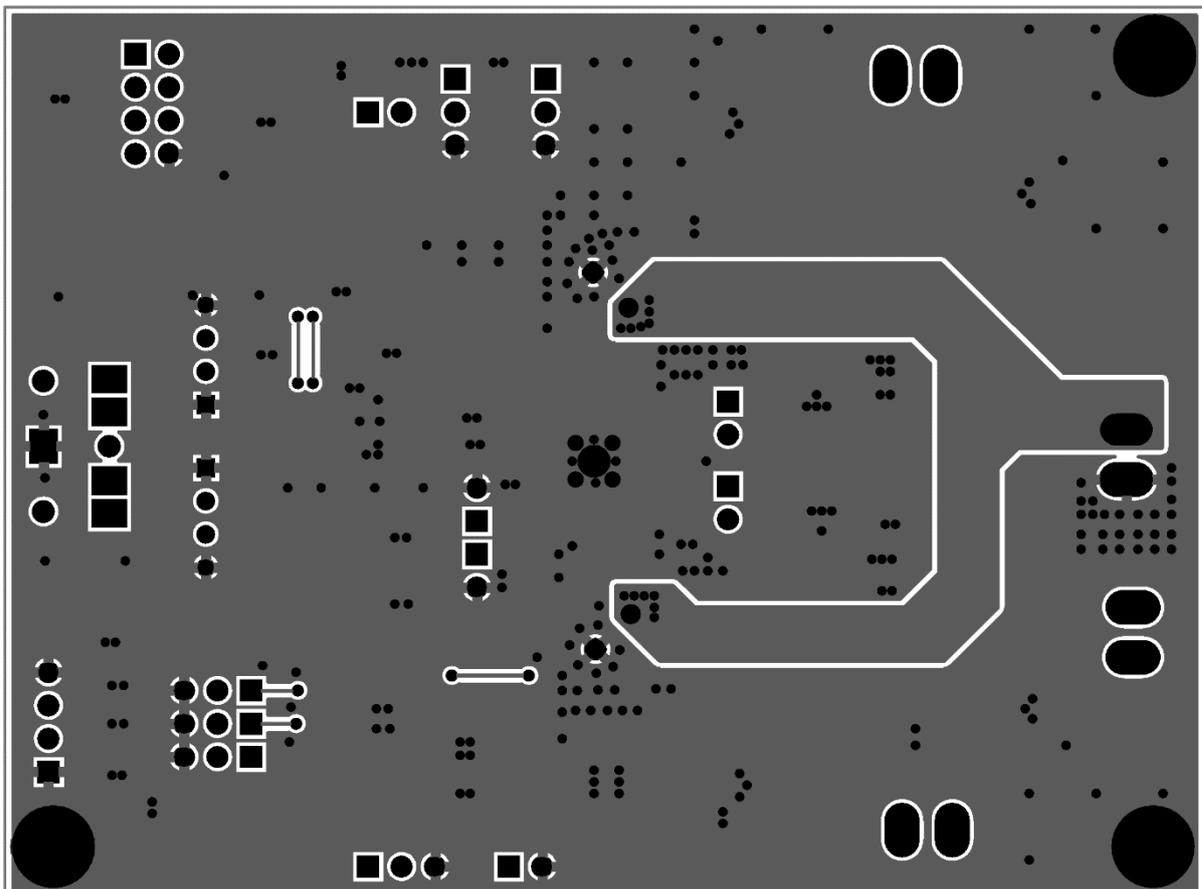
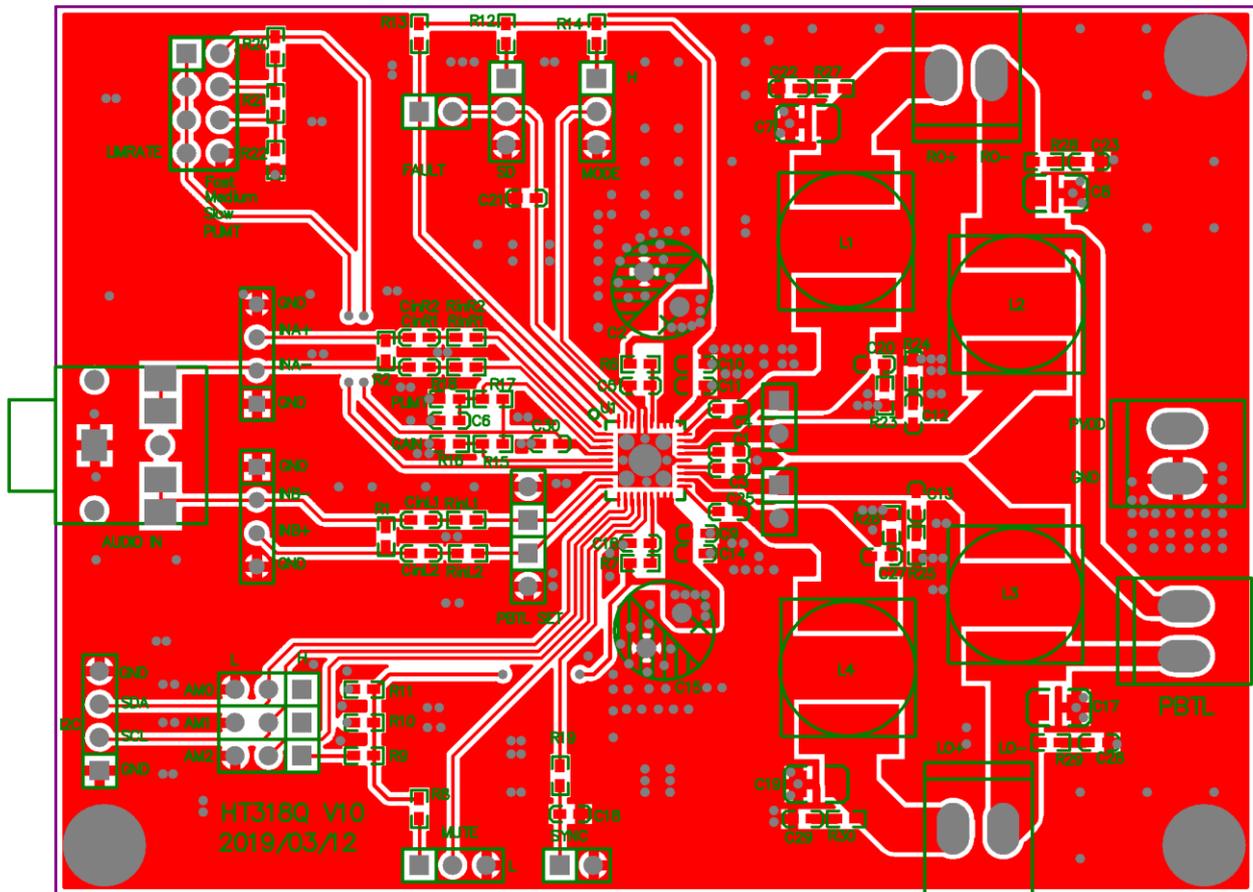
9.5 Under-Voltage Protection (UVP)

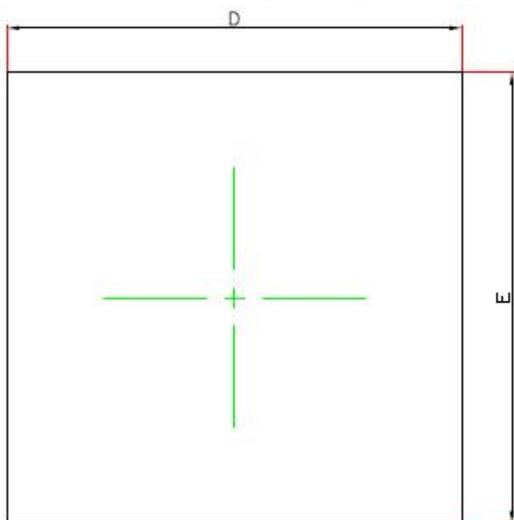
This is the function to establish the under-voltage protection mode when power supply becomes lower than the detection voltage V_{UVLL} , and the protection mode is canceled when the power supply becomes higher than the threshold voltage V_{UVLH} . In the under-voltage protection mode, the differential output pin becomes weak low state (a stage grounded through resistivity). HT318 will start up within start-up time when the under-voltage protection mode is cancelled.

10. Typical Applications

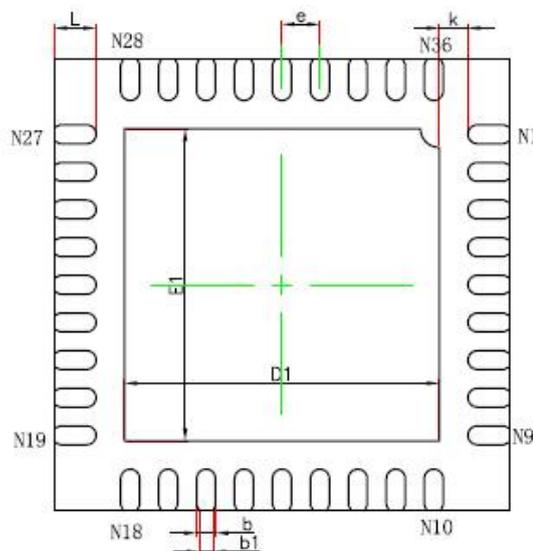


11. PCB Layout

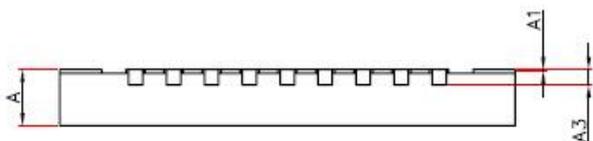


PACKAGE OUTLINE
QFN36L 6*6 with exposed thermal pad


TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	5.900	6.100	0.232	0.240
E	5.900	6.100	0.232	0.240
D1	4.050	4.250	0.159	0.167
E1	4.050	4.250	0.159	0.167
b	0.180	0.300	0.007	0.012
b1	0.130	0.230	0.005	0.009
e	0.500TYP.		0.020TYP.	
k	0.200MIN.		0.008MIN.	
L	0.500	0.600	0.020	0.024

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