带有3.3V, 150mA LDO输出的100V输入，3.5A开关限流降压变换器

100V Input, 3.5A, Switching Current Limit Step-Down Converter with a 3.3V, 150mA LDO

■ FEATURES

- Wide 5V to 100V Input Range
- 3.5A Typical Peak Switching Current Limit
- Integrated a 3.3V, 150mA LDO
- Hysteretic Control: No Compensation
- Up to 1MHz Switching Frequency
- Short-Circuit Protection (SCP) with Integrated High-Side MOSFET
- 200μA Quiescent Current
- Thermal Shutdown
- Packages: Pb-free Packages, ESOP8

- 宽输入电压: 5V – 100V
- 峰值开关电流限值典型3.5A
- 内置3.3V, 150mA LDO
- 滞后电压控制模式，无需补偿
- 最高1MHz开关频率
- 集成高端MOSFET的短路保护
- 200μA静态电流
- 过热关断保护
- ESOP8封装

■ APPLICATIONS

- Scooters, E-Bike Control Power Supplies
- Solar Energy Systems
- Automotive System Power
- Industrial Power Supplies
- High-Power LED Drivers
- GPS Trackers

- 电动车控制电源
- 汽车系统电源
- 大功率LED驱动器
- 太阳能系统
- 工业电源
- GPS追踪器

■ DESCRIPTION

The HT7887 is a high-voltage, step-down, switching regulator that delivers up to 2A of continuous current to the load. It integrates a high-side, high-voltage, power MOSFET with a current limit of 3.5A, typically. The wide 5V to 100V input range accommodates a variety of step-down applications, making it ideal for automotive, industry, and lighting applications. Hysteretic voltage-mode control is employed for very fast response. The HT7887 also integrates a 150mA LDO which can provide 3.3V power rail for the system.

The switching frequency can be up to 1MHz, allowing for small component size. Thermal shutdown and short-circuit protection (SCP) provide reliable and fault-tolerant operations. A 200μA quiescent current allows the HT7887 to be used in battery-powered applications.

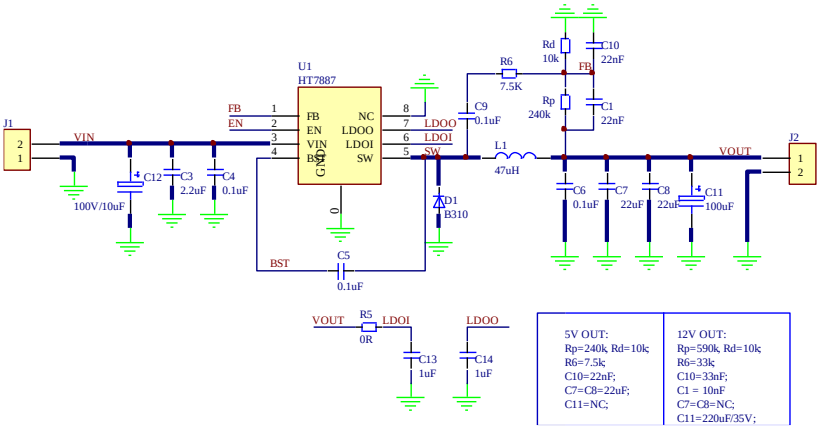
The HT7887 is available in ESOP8 package.

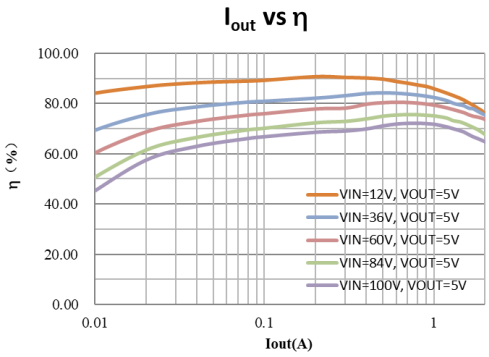
HT7887是一款高压降压开关稳压器，可向负载提供高达2A的连续电流。它集成了高压的高端功率MOSFET，电流限制通常为3.5A。其极宽的5V至100V输入电压范围能适应各种降压应用，使其成为汽车、工业和照明应用的理想选择。迟滞电压模式控制的应用，使其具有良好的瞬态响应能力。HT7887集成了一个输出3.3V, 150mA的LDO。

开关频率可高达1MHz，从而允许小尺寸的外围器件。过热保护和短路保护（SCP）使芯片具有较好的可靠性和容错机制。200μA的静态电流允许HT7887用于电池供电的应用中。

该产品提供ESOP8封装。

■ TYPICAL APPLICATION





关于 HT7887 的注意事项

HT7887 的输出电容（C_{OUT}）是实现平滑输出电压所必需的，并且对其 ESR 有较为严格的要求。如规格书所述，输出电容的 ESR 应足够大，否则，系统可能会以意外的方式运行，并且电流纹波可能非常高。一般建议的输出电容器 ESR 范围为 100mΩ至 250mΩ，在整个工作条件、工作温度范围内。具体选择如下：

（1） 使用陶瓷电容或电解电容（推荐方式）

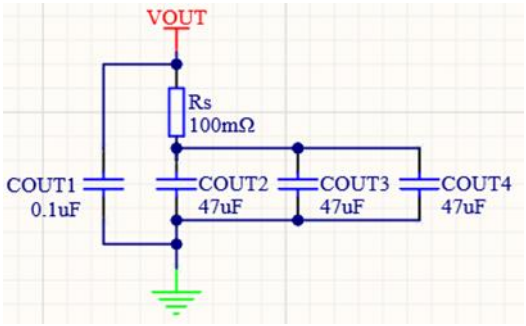
使用陶瓷电容或电解电容器时，FB 通过正向电阻、电容（C9 和 R6）连接到 SW，如典型应用图。通过调整 R6 和 C10 的值，可以改变 SW 的频率，$f_{SW} \propto \frac{1}{R_6 C_{10}}$，即增大 R6 或 C10，fsw 减小。建议 fsw 设置在约 200kHz~300kHz。

（2） 选择使用钽电容

输出电容使用 0.1uF + 2.2uF +100uF 钽电容的并联组合， 钽电容可使用 593D107X9010C2T3 或类似型号，其标称的 ESR 为 200mΩ

（3） 使用陶瓷电容并联电阻

由于钽电容价格昂贵，更多客户倾向于使用廉价的电解电容或陶瓷电容。由于电解电容的温度特性较差，一般不建议使用。使用陶瓷电容时，其 ESR 较小，不足以提供足够的 ESR 以使 HT7887 稳定运行，需要在陶瓷电容上串联一个电阻 Rs（100~250mΩ），且后级没有更多电容（更多电容会同步影响 ESR），如下图：



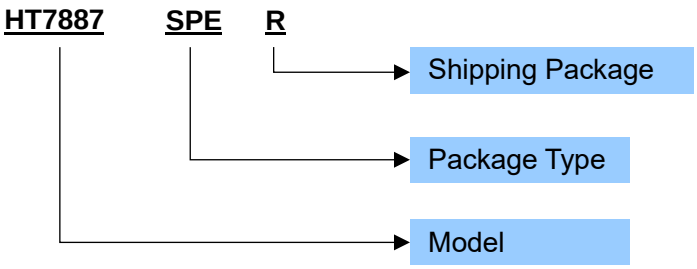
HT7887 Layout 建议

（1）将输入电容器、二极管和 HT7887（VIN、SW 和 PGND）尽可能靠近；
（2）输入电容建议至少放置一个电解电容（至少 10uF，耐压≥输入最高电压*1.5）；
（3）保持电源轨迹非常短且相当宽，特别是对于 SW 节点。
这有助于大大降低 SW 节点上的电压尖峰，并降低 EMI 噪声水平。
（4）FB 走线尽可能远离电感和功率走线（如 SW 节点）。
（5）将直径为15mil、间距为40mil（中心之间的距离）的热通孔放置在裸露的焊盘下方，以改善热传导。

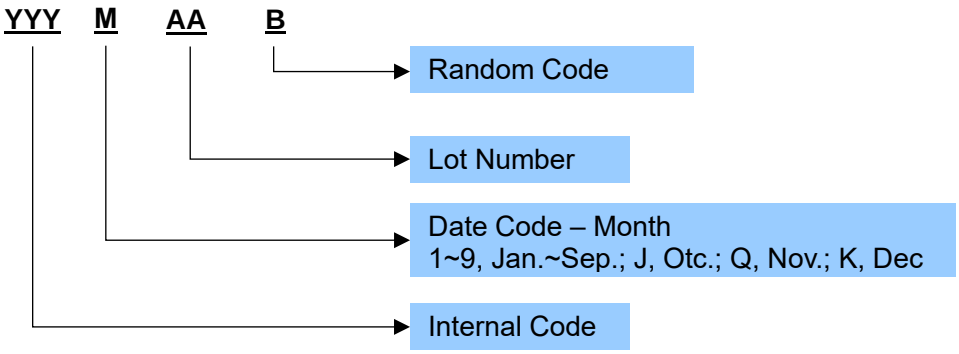
■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	Shipping Package / MOQ
HT7887SPER	ESOP8 (SPE)	HT7887SP YYYMAAB[1]	-40℃～125℃	Tape and Reel / 2500pcs

Part Number

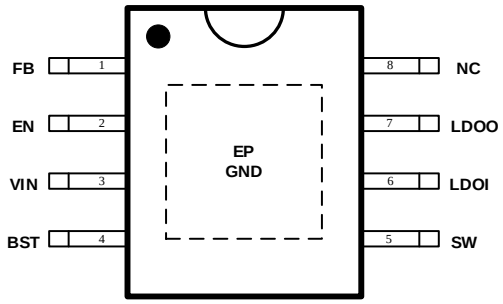


Production Tracking Code



[1] YYYMAAB is production tracking code

■ TERMINAL CONFIGURATION



Top View

■ TERMINAL FUNCTION

Terminal No.	Name	Description
1	FB	Feedback. FB is the input to the voltage hysteretic comparators. The average FB voltage is maintained at 200mV by loop regulation. 反馈。FB是电压迟滞比较器的输入。通过环路调节， FB电压保持在平均200mV
2	EN	Enable input. Pull EN below the specified threshold to shut down the HT7887. Pull EN above the specified threshold or leave EN floating to enable the HT7887. 使能脚。将EN拉到阈值以下以关闭HT7887。将EN拉至阈值以上或悬空，以启用HT7887。
3	VIN	Input supply for the buck. VIN supplies power to all of the internal control circuitries, both BST regulators, and the high-side switch. A decoupling capacitor to ground must be placed close to VIN to minimize switching spikes. 降压的输入电源。VIN为所有内部控制电路、BST调节器和高端管供电。接地滤波电容必须放置在VIN附近，以减少开关尖峰
4	BST	Bootstrap. BST is the positive power supply for the internal, floating, high-side MOSFET driver. Connect a bypass capacitor between BST and SW. BST是内部高端MOSFET驱动器的正电源。在BST和SW之间连接一个旁路电容器。
5	SW	Switch node. SW is the output from the high-side switch. A low forward voltage Schottky rectifier to ground is required. The rectifier must be placed close to SW to reduce switching spikes. SW是高短管的输出。需要接低正向电压的肖特基二极管到地。二极管必须靠近SW，以减少开关尖峰
6	LDOI	Input supply for internal LDO, connect to VOUT. LDO的输入电源，可连接至VOUT。
7	LDOO	Output of LDO, at least a 1uF ceramic cap should be connected. LDO输出，接1uF滤波器。
8	NC	No connection, connect to GND or floating. 内部无连接，外部接地或悬空。
EP	GND	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder. For proper electrical operation, this ground pad must be connected to the system ground. 既是地，又是散热PAD

■ SPECIFICATIONS[1]

● Absolute Maximum Ratings [2]

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Power supply voltage for VIN	VIN	-0.3		100	V
Power supply voltage for VIN, transient <100ns		-0.3		120	V
Power supply voltage for LDOI	V_{LDOI}	-0.3		36V	
Switch voltage	SW	-0.5 (-7V for 10ns)		VIN+0.5	V
BST to SW		-0.3		6	V
All other pins		-0.3		6	V
Moisture Sensitivity Level (MSL)			MSL3		
Ambient Operating Temperature	T_A	-40		125	℃
Junction Temperature	T_J	-40		150	℃
Storage Temperature	T_{STG}	-65		150	℃

● Recommended Operating Conditions

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage for VIN	VIN		5		95	V
Power supply voltage for LDOI	V_{LDOI}		3		30	V
EN voltages			0		5	V
Maximum switching frequency	fsw				1M	Hz
Ambient Operating Temperature	T_a		-40		125	℃

● Electrical Characteristics

VIN = 60V, TA = +25°C, unless otherwise noted. Specifications over temperature are guaranteed by design and characterization.

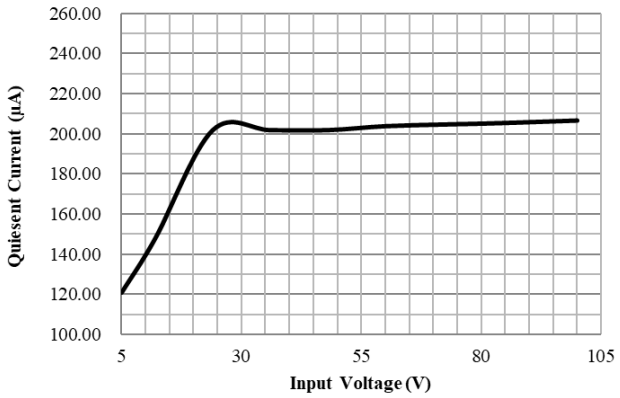
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
VIN UVLO threshold	V_{UVLO}			4.7		V
VIN UVLO hysteresis	V_{hys}			0.3		V
Shutdown supply current	I_{SD}	V_{EN} = 0V		5		μA
Quiescent supply current	I_Q	No load, V_{FB} = 250mV, from VIN pin		200		μA
		From LDOI pin		2		uA
Upper switch on resistance	$R_{DS(ON)}$	V_{BST} - V_{SW} = 5V		380		mΩ
Upper switch leakage current	I_{SWLK}	V_{EN} = 0V, V_{SW} = 0V		0.01		μA
Current limit	I_{PK}	V_{FB} = 150mV, HT7887		3.5		A
EN up threshold	V_{ENH}			1.8		V
EN threshold hysteresis	V_{ENHY}			400		mV
EN input current	I_{ENI}	VEN = 5V		0.01		μA
EN pull-up current	I_{ENS}	EN = 2V		2		μA
LDO Output voltage	V_{LDOO}			3.3		V
LDO current limit	ILDO		150			mA
Load regulation				0.05		%
Feedback voltage threshold high	V_{FBH}	4.5V < VIN < 95V, V_{FB} rising from 0V until V_{SW} < 30V		215		mV
Feedback voltage threshold low	V_{FBL}	4.5V < VIN < 95V, VFB falling from 0.25V until VSW > 30V		185		mV
FB input current	I_{FB}	VFB = 5V or 0V	-300		300	nA

[1] Depending on parts and PCB layout, characteristics may be changed.
[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

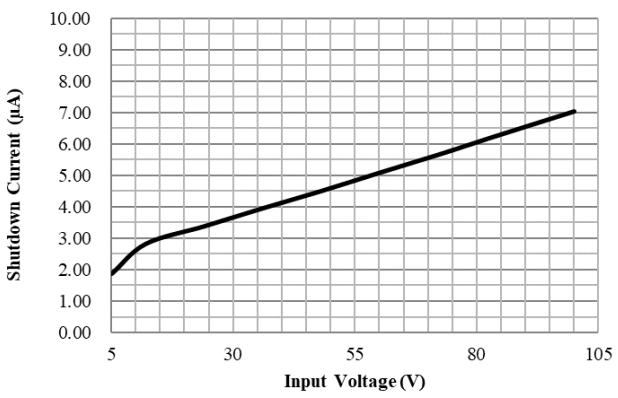
FB propagation delay to output high	T_{FBDH}	Falling edge of VFB from 0.25V to 0V to V_{SW} rising edge		100		ns
FB propagation delay to output low	T_{FBDL}	Rising edge of VFB from 0V to 0.25V to V_{SW} falling edge		100		ns
Thermal shutdown		Trigger thermal shutdown		150		℃
		Hysteresis		20		℃

■ TYPICAL OPERATING CHARACTERISTICS

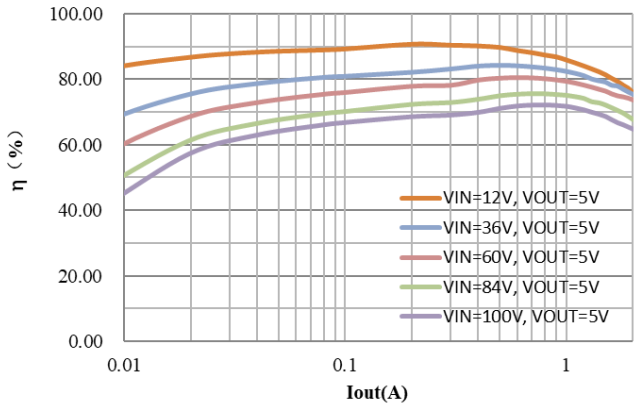
Quiesent Current vs Input Voltage



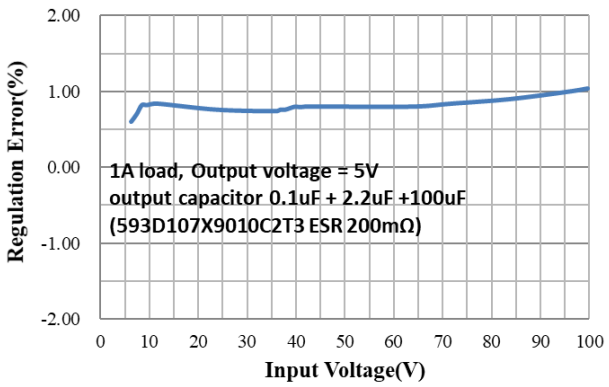
Shutdown Current vs Input Voltage



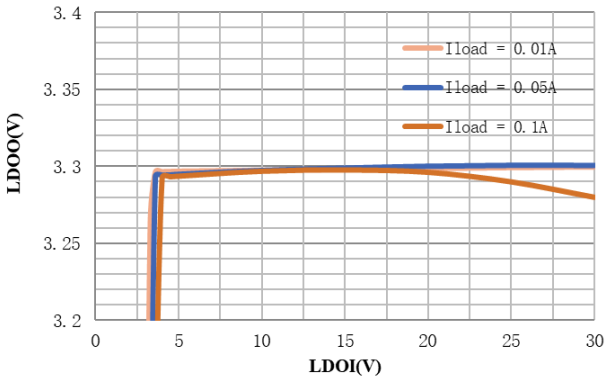
I_{out} vs η



Line Regulation



LDOO vs LDOI



■ APPLICATION INFORMATION

1 Hysteresis Current Control with Adaptive Threshold Adjustment

The HT7887 operates in a hysteretic voltage-control mode to regulate the output voltage. FB is connected to the tap of a resistor divider, which determines the output voltage. The power MOSFET is turned on when the FB voltage (V_{FB}) drops to 185mV and remains on until V_{FB} rises to 215mV. The power MOSFET is turned off when V_{FB} rises to 215mV and remains off until V_{FB} falls to 185mV. The two thresholds of 215mV and 185mV are adjusted adaptively to compensate for all the circuit delays, so the output voltage is regulated with an average 200mV value at FB.

HT7887 在滞后电压控制模式下工作，以调节输出电压。FB 连接到电阻分压器的中间，电阻分压器决定输出电压。当 FB 电压（V_{FB}）降至 185mV 时，功率 MOSFET 开启，并保持开启状态，直到 V_{FB} 升至 215mV。当 V_{FB} 上升到 215mV 时，功率 MOSFET 关闭，并保持关闭状态，直到 V_{FB} 下降到 185mV。215mV 和 185mV 的两个阈值自适应调整，以补偿所有电路延迟，因此输出电压在 FB 处以平均 200mV 值调节。

2 Enable (EN) Control

The HT7887 has a dedicated enable control pin (EN) with positive logic. Its falling threshold is 1.3V, and its rising threshold is 1.7V.

When floating, EN is pulled up to about 2.5V by an internal 2μA current source, so it is enabled. A current over 2μA is needed to pull EN down.

HT7887 的 EN 脚高电平有效，控制芯片使能。其下降阈值为 1.3V，上升阈值为 1.7V。

悬空时，EN 被内部 2μA 电流源拉高至约 2.5V，芯片使能。需要超过 2μA 的电流才能将 EN 下拉。

3 Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own under-voltage lockout (UVLO) protection. The UVLO rising threshold is 2.2V with a hysteresis of 150mV.

The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator.

功率 MOSFET 驱动由外部自举电容器供电。该功率管有其自身的欠压锁定（UVLO）保护。UVLO 上升阈值为 2.2V，磁滞 150mV。

内部自举调节器通过外部自举电容充电调节至约 5V。

4 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at an insufficient supply voltage. The UVLO rising threshold is about 4.7V, while its falling threshold is a consistent 4.4V.

欠压锁定（UVLO）功能可避免芯片工作在电源电压不足的条件。UVLO 上升阈值约为 4.7V，下降阈值为 4.4V。

5 LDO

The HT7887 integrated a 150mA LDO that can provide a 3.3V power supply. The input supply voltage of the LDO is LDOI, and the output voltage of the LDO is LDOO. Only when the LDOI voltage is dropped below 3V can the LDO be disabled.

The LDOI can be connected to VOUT or external power supply. If the LDOI is connected to VOUT, make sure that the VOUT is set in the recommneded LDOI voltage. If LDOI is connected to an external power supply, the LDO can work singly even if the buck is disabled.

Filtering capacitors should be placed as close to the device as possible for both LDOI and LDOO.

HT7887 内置了一个 150mA LDO，其可输出 3.3V 电压。该 LDO 的输入是 LDOI，输出是 LDOO。只有档 LDOI 的电压低于 3V 时，LDO 才会关闭。

LDOI 可连接至 VOUT，也可接到外部供电。接到 VOUT 时，注意将 VOUT 设置在 LDOI 推荐电压范围内；若 LDOI 接到外部电压，LDO 可独立工作，即使降压处于关闭状态。

LDOI 和 LDOO 均需要连接滤波电容，以确保稳定性。

6 Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than its upper threshold, the entire chip shuts down. When the temperature is lower than its lower threshold, the chip is enabled again.

过热关断保护是为了防止芯片在极高的温度下工作。当芯片温度高于其上限阈值时，整个芯片关闭。当温度低于其下限阈值时，芯片再次启用。

7 Output Short Protection

For the buck, the output voltage is well-regulated when V_{FB} is around 200mV. If the output is pulled low in over-current protection (OCP) or is shorted to GND directly, V_{FB} is low, even though the power MOSFET is turned on. The HT7887 regards the low V_{FB} as a failure. The power MOSFET shuts off if the failure time is longer than 10µs. The HT7887 attempts operation again after a delay of about 300µs.

The power MOSFET current is also accurately sensed via a current sense MOSFET. If the current is over the current limit, the IC is shut down. This offers extra protection under output-short conditions.

For the LDO, when the output current of LDOO is higher than LDO current limit or the LDOO is short to GND, the output short protection is triggered and the output current is clamped at 80mA to avoid theraml damage.

对于芯片降压部分，当 V_{FB} 在 200mV 左右时，输出电压被稳定调节。如果输出在过电流保护（OCP）中拉低或直接对 GND 短路，则 V_{FB} 低，即使功率 MOSFET 开启。HT7887 将低 V_{FB} 视为故障。如果故障时间超过 10µs，功率 MOSFET 将关闭。HT7887 在大约 300µs 的延迟后再次尝试工作。

功率 MOSFET 电流通过电流检测 MOSFET 精确检测。如果电流超过电流限制，IC 将关闭。这在输出短路条件下提供了额外的保护。

对于 LDO 部分，当 LDOO 引脚的输出电流高于电流限制阈值或 LDOO 对 GND 短路时，将触发短路保护，输出电流将被箝位至约 80mA，以防止温度过高造成芯片损坏。

8 Setting the Output Voltage

The output voltage (V_{OUT}) is set by a resistor divider (R1 and R2) (see the Typical Application on page 2). The resistor divider can be determined with following Equation.

$$R1 = \frac{V_{OUT} - V_{FB}}{V_{FB}} \times R2$$

Where V_{FB} is 0.2V, typically.

输出电压（V_{OUT}）由电阻分压器（R1 和 R2）设置（参见第 2 页的典型应用）。可以使用以下公式确定电阻。

$$R1 = \frac{V_{OUT} - V_{FB}}{V_{FB}} \times R2$$

其中，V_{FB} 的典型值为 0.2V。

9 Output Capacitor and Frequency Setting

The output capacitor (C_{OUT}) is necessary for achieving a smooth output voltage. The ESR of the capacitor should be sufficiently large compared to the capacitance; otherwise, the system may behave in an unexpected way, and the current ripple may be very high. V_{FB} changes from 185mV to 215mV when the power MOSFET switches on. To charge the capacitor and generate 215mV at FB, the system needs ESR and some inductor current. For example, for a 5V V_{OUT}, if the forward capacitor is 0.1µF, the suggested ESR range of the output capacitor is 100mΩ to 250mΩ. Tantalum or aluminum electrolytic capacitors with a small ceramic capacitor are recommended.

A forward capacitor across R1 is recommended when the output capacitor is tantalum or aluminum electrolytic, which can set the desired frequency if the output capacitor and ESR cannot be changed. The forward capacitor can reduce the output voltage ripple.

In some application, simply a forward capacitor may not get proper frequency, then we can add a forward resistor in series with the forward capacitor or even more add a ceramic on the output.

输出电容（C_{OUT}）是实现平滑输出电压所必需的。与电容值相比，电容的 ESR 应足够大；否则，系统可能会以意外的方式运行，并且电流纹波可能非常高。当功率 MOSFET 打开时，V_{FB} 从 185mV 变为 215mV。为了给电容器充电并在 FB 处产生 215mV，系统需要 ESR 和一些电感电流。例如，对于 5V V_{OUT}，如果正向电容器为 0.1µF，建议的输出电容器 ESR 范围为 100mΩ至 250mΩ。建议使用小型陶瓷电容并联钽或铝电解电容。

当输出电容为钽或铝电解电容时，建议在 R1 上并联正向电容器，其在不能改变输出电容和 ESR 时可设置所需开关频率。该正向电容可以降低输出电压纹波。

在某些应用中，单一的正向电容器可能无法获得合适的开关频率，则可以添加一个正向电阻与正向电容器串联，或甚至在输出端添加一个陶瓷电容。

10 Selecting the Inductor

The inductor (L) is required to convert the switching voltage to a smooth current to the load. Although the output current is low, it is recommended that the inductor current be continuous in each switching period to prevent reaching the current limit. Calculate the inductor value with the following Equation.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{F_{SW} \times I_{OUT} \times V_{IN} \times K}$$

电感器（L）需要将开关电压转换为平滑的负载电流。虽然输出电流较低，但建议在每个开关周期内电感电流保持连续，以防止达到电流限制。可使用以下公式计算电感器值。

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{F_{SW} \times I_{OUT} \times V_{IN} \times K}$$

Where K is a coefficient of about 0.15 ~ 0.85.

其中系数 K 约为 0.15~0.85。

11 Output Rectifier Diode

The output rectifier diode supplies current to the inductor when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky diode.

当高压侧开关断开时，输出整流二极管向电感器提供电流。为了减少二极管正向电压和恢复时间造成的损耗，请使用肖特基二极管。

The average current through the diode can be approximated with the following Equation:

通过二极管的平均电流可通过以下公式计算：

$$I_D = I_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Choose a diode with a maximum reverse voltage rating greater than the maximum input voltage and a current rating is greater than the average diode current.

选择最大反向电压额定值大于最大输入电压且额定电流大于平均二极管电流的二极管。

12 Input Capacitor (C_{IN})

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance, especially under high switching frequency applications.

降压转换器的输入电流是不连续的，因此需要一个电容向降压转换器提供交流电流，同时保持直流输入电压。使用低 ESR 电容以获得最佳性能，尤其是在高开关频率应用下。

The RMS current through the input capacitor can be calculated with the following Equation:

通过输入电容的 RMS 电流可通过以下公式计算。

$$I_{IN\_AC} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

With low ESR capacitors, the input voltage ripple can be estimated with the following Equation.

对于低 ESR 电容，输入电压纹波可通过以下方程式估算

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{OUT}}{F_{SW} \times C_{IN} \times V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Choose an input capacitor with enough RMS current rating and enough capacitance for small input voltage ripples.

选择一个具有足够的 RMS 电流额定值和足够容值的电容作为输入电容，以实现较小的输入电压纹波。

When electrolytic or tantalum capacitors are applied, a small, high-quality ceramic capacitor (i.e.: 0.1μF) should be placed as close to the IC as possible.

当使用电解电容或钽电容时，应将小型优质陶瓷电容（即：0.1 μ F）放置在尽可能靠近 IC 的位置。

13 PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 1 and follow the guidelines below.

(1) Place the input decoupling capacitor, output rectifier diode, and the HT7887 (VIN, SW, and PGND) as close to each other as possible.

(2) Keep the power traces very short and fairly wide, especially for the SW node.

This can help greatly reduce voltage spikes on the SW node and lower the EMI noise level.

(3) Run the feedback trace as far from the inductor and noisy power traces (like the SW node) as possible.

(4) Place thermal vias with 15mil barrel diameter and 40mil pitch (distance between the centers) under the exposed pad to improve thermal conduction.

有效的 PCB 布局对于稳定运行至关重要。要获得最佳结果，请参考图 1 并遵循以下指南。

（1）将输入电容器、二极管和 HT7887（VIN、SW 和 PGND）尽可能靠近。

（2）保持电源轨迹非常短且相当宽，特别是对于 SW 节点。

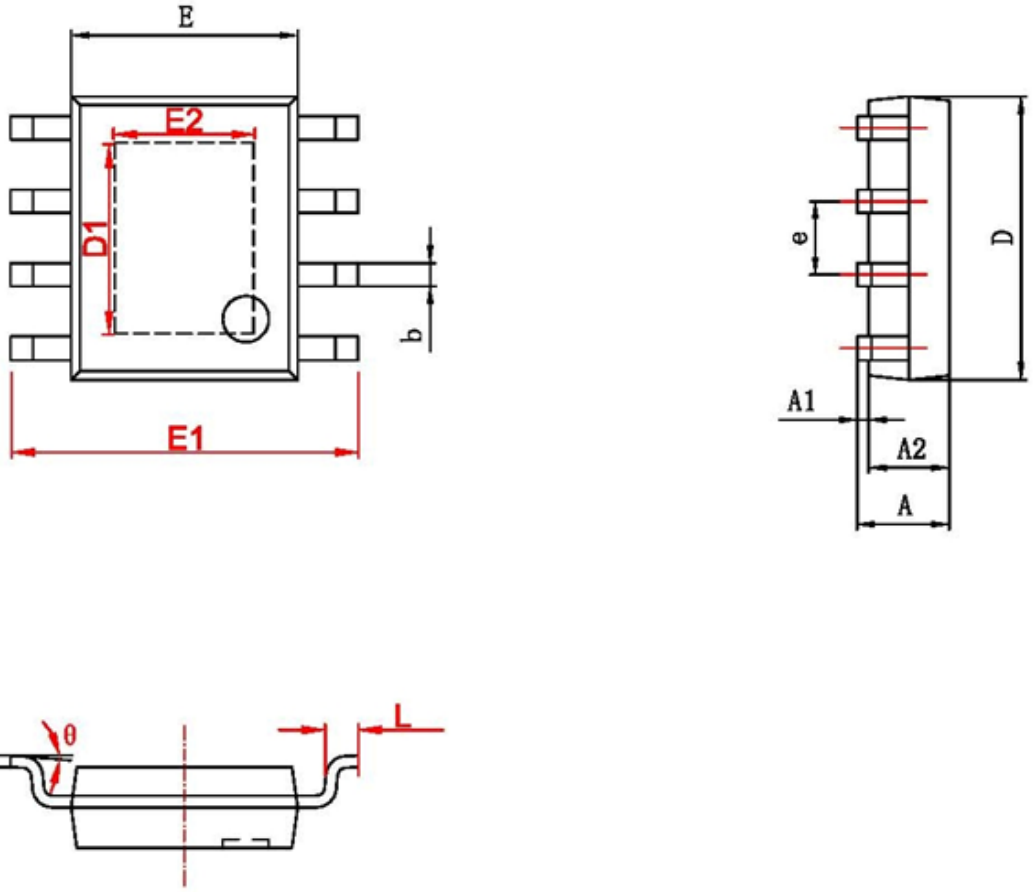
这有助于大大降低 SW 节点上的电压尖峰，并降低 EMI 噪声水平。

（3）FB 走线尽可能远离电感和功率走线（如 SW 节点）。

（4）将直径为 15mil、间距为 40mil（中心之间的距离）的热通孔放置在裸露的焊盘下方，以改善热传导。

■ PACKAGE OUTLINE

SPE (ESOP8)



Symbol	Dimensions in Millimeters Choice 1 (B)		Dimensions in Millimeters Choice 2 (T)	
	Min.	Max.	Min.	Max
A	1.3	1.7	1.35	1.55
A1	0.00	0.10	0.00	0.10
D	4.70	5.10	4.70	5.10
E	3.80	4.00	3.80	4.00
E1	5.80	6.20	5.80	6.20
D1	3.05	3.25	3.3 REF	
E2	2.16	2.36	2.4 REF	
b	0.33	0.51	0.30	0.45
c	0.17	0.25	0.18	0.22
e	1.27TYP.		1.27TYP.	
L	0.40	1.27	0.40	0.80
θ	0°	8°	0°	8°

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