

5V~130V输入, 超低静态功耗, 0.7A同步降压变换器, 支持隔离降压拓扑

130V Input, 0.7A, Ultra-Low IQ, Synchronous Buck Converter with ISO-Buck Capability

FEATURES

Low R_{DS(ON)} for internal MOSFETS

(1.8 Ω /700m Ω), diode emulation for high light-load efficiency

- Wide input voltage range: 5V~130V
- Continuous output current: 0.7A
- Ultra-Low IQ: 10uA; 3µA shutdown current
- Nearly 100% duty cycle if needed

• PFM (HTN77A0P) or FPWM (HTN77A0F) in light load

· FPWM enables ISO-Buck capability

- Up to 1MHz Programmable Switching
 Frequency
- Open drain PG pin as power good flag
- COT mode control
- · Peak and valley current-limit protection
- Under-voltage and Over-Temperature
 Protection
- Packages: Pb-free Packages, ESOP8

- ·内置1.8Ω/700mΩ高低端功率管,无需外部续流
- 二极管,轻载高效率
- · 宽输入电压范围: 5V~130V
- ・输出最大持续电流: 0.7A
- ・超低静态电流: 10uA; 3uA关断电流
- ·可接近100%占空比工作
- ・脉冲跳跃模式使得轻载下高效率(HTN77A0P), 或 强制PWM(HT77A0F)
- ·FPWM支持隔离降压拓扑
- ·最高1MHz可编程开关频率
- ·开漏的PG pin,指示输出电压正常
- ・COT控制架构
- ・峰值和谷值限流保护
- ・欠压保护和过热关断保护
- ・无铅封装, ESOP8

APPLICATIONS

- Brick power module
 Battery pack
- HV battery
 Industrial Power Supplies
- Automotive System

- ・ 砖块电池模组 いいも 电池包
- 高压电池组・・・エ业电源
- ・ 汽车系统



TYPICAL APPLICATION

Buck应用



1. CIN电容典型使用1uF~2.2uF电容,应尽可能靠近VIN和GND脚,电容额定电压需大于最大输入电压。输

入有插拔毛刺时,可增加≥10uF的电解电容减小毛刺,确保最高电压不超过130V。

2. EN设置:

EN<0.45V	芯片关闭
EN=1.1~1.3V	芯片进入Standby模式
EN>1.5V	芯片进入正常工作状态

3. RT设置频率: $fsw(kHz) = \frac{2500*VOUT(V)}{DT(L_{2})}$ $RT(k\Omega)$

4. 设置电压*VOUT* =
$$1.2 * (1 + \frac{Rp}{Pd})$$

5. PG不使用时,可悬空或接地; PG使用时,通过47k电阻上拉至<14V的电压,并向外输出高低状态。

PG=L	V _{FB} <0.9*VREF, 输出电压不稳
PG=Hi-Z, (外部通过47k电阻上拉至<14V的电压,	V _{FB} >0.95*VREF, 输出电压稳定
则输出为高)	

6. BST电容CBOOT典型使用2.2nF;

7. 电感典型使用68uH (fsw设置为500kHz时), 饱和电流建议大于1.4*最大输出电流;

8. 输出电容: 2*22uF(陶瓷), 额定耐压大于VOUT 2倍以上;

9. 相关推荐参数设置:

	Rp	Rd	RA	CA	СВ	RT
VOUT = 5V	470k	150k	120k	3.3nF	100pF	24.9k (fsw≈500kHz)
VOUT =12V	200k	22k	120k	3.3nF	100pF	62k (fsw≈500kHz)

10. R_P和C_A应连接至Cout滤波后。



ISO-Buck应用



1. C_{IN}电容典型使用1uF~2.2uF电容,应尽可能靠近VIN和GND脚,电容额定电压需大于最大输入电压。输入有插拔毛刺时,可增加≥10uF的电解电容减小毛刺,确保最高电压不超过130V。

2. EN设置:

EN<0.45V	芯片关闭
EN=1.1~1.3V	芯片进入Standby模式
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3. RT设置频率: $fsw(kHz) = \frac{2500*VOUT(V)}{RT(k\Omega)}$

4. 设置电压VOUT = $1.2 * (1 + \frac{Rp}{Rd})$

5. PG不使用时,可悬空或接地; PG使用时,通过47k电阻上拉至<14V的电压,并向外输出高低状态。

PG=L	V _{FB} <0.9*VREF, 输出电压不稳
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则输出为高)	

6. BST电容CBOOT典型使用2.2nF;

7. 变压器典型使用68uH (fsw设置为500kHz时), 饱和电流建议大于1.4*最大输出电流; 匝数比

$$\frac{N2}{N1} \approx \frac{VOUT2}{VOUT}$$

8. 输出电容:

非隔离端输出电容Cout: 2*22uF(陶瓷), 额定耐压大于VOUT 2倍以上;

隔离端输出电容Cout2: 2*22uF(陶瓷), 额定耐压大于VOUT 2倍以上;

9. D1反向额定电压*V_{RMS} > V_{IN} × ^{N2}/_{N1} + VOUT2*,额定电流>最大输出电流,可典型使用使用SS120 (200V, 1A) 10. 相关推荐参数设置:

	Rp	Rd	RA	CA	СВ	RT
VOUT = 5V	470k	150k	120k	3.3nF	100pF	24.9k (fsw≈500kHz)
VOUT =12V	200k	22k	120k	3.3nF	100pF	62k (fsw≈500kHz)

11. RP和CA应连接至Cout滤波后。



DESCRIPTION

The HTN77A0 is a synchronous buck converter with wide input voltage, ranging from 5V to 130V, which integrates a 1.8Ω high-side MOSFET and a 0.7 Ω low-side MOSFET. With 0.84A peak current limit, the device can deliver up to 0.7A continuous output current.

The HTN77A0, adopting the constant on-time control, supports the Pulse Frequency Modulation (PFM) which assists the converter on achieving high efficiency at light load, while HTN77A0F works in forced PWM mode at light load.

The HTN77A0 features programmable switching frequency from 100kHz to 1MHz with an external resistor.

The HTN77A0 allows power conversion from high input voltage to low output voltage with a minimum 50ns on-time of switch MOS. The device offers fixed 3ms soft start to prevent inrush current during the startup. The HTN77A0 features external loop compensation to provide the flexibility to optimize either loop stability or loop response.

The HTN77A0 provides valley current limit, peak current limit, thermal shutdown protection, and input voltage under-voltage protection. The device is available in an ESOP8 package.

HTN77A0是一个同步降压转换器,具有从 5V到130V的宽输入电压,集成了1.8Ω高侧 MOSFET和0.7Ω低端MOSFET。器件带有 0.84A峰值限流,可输出持续0.7A。

HTN77A0采用基于恒定导通时间(COT) 控制架构,支持跳周期调制(PFM),有助于 转换器在轻负载下实现高效率;HTN77A0F则 在轻载时仍工作在强制PWM。

HTN77A0具有100kHz至1MHz的可编程 开关频率,外部电阻可调。

HTN77A0允许从高输入电压到低输出电 压的功率转换,开关MOS的最小导通时间为 50ns。该器件提供3ms的固定软启动,以防止 启动过程中的涌入电流。HTN77A0具有外部环 路补偿功能,可灵活优化环路稳定性或环路响 应。

HTN77A0提供谷值电流限制、峰值电流限 值、热关断保护和输入电压欠压保护。该器件 采用ESOP8封装。





ORDERING INFORMATION

Part Number	Package Type	Package Abbr.	Eco Plan	Working mode at light load	MSL Level	Marking	Shipping Package / MOQ
HTN77A0PSPER	ESOP8	SPE	RoHS	PFM	MSL3	HTN77A0 YYYMAAB ¹	Tape and Reel (R) / 2500pcs
HTN77A0FSPER	ESOP8	SPE	RoHS	FPWM	MSL3	HTN77A0 YYYMAAB	Tape and Reel (R) / 2500pcs

Part Number



Production Tracking Code





■ TERMINAL CONFIGURATION



■ TERMINAL FUNCTION

Terminal No.	Name	Description
1	GND	Ground 芯片地
2	VIN	Voltage input terminal. 芯片电源输入。
3	EN	 Enable pin to the regulator with internal pull-up current source. Pull low to disable the converter. Float or connect to HIGH to enable the converter. 稳压器使能引脚,带内部上拉电流源。将端口拉低以禁用转换器。悬空或连接到逻辑高电平可以启动转换器。
4	RT	Set the internal oscillator clock frequency. Connect a resistor from this pin to ground to set switching frequency. 设置内部振荡器时钟频率。将一个电阻器从该引脚连接到地,以设置开关频率。
5	FB	Feedback. Connect resistor divider to output voltage. 反馈。接分压电阻到输出电压。
6	PG	Power good. 输出电源信号建立标志。
7	BST	Bootstrap. Power supply for the high-side MOSFET driver. Connect a bypass capacitor between BST and SW. BST是内部高端MOSFET驱动器的正电源。在BST和SW之间连接一个旁路电容器。
8	SW	Switch node, Connect SW to an external power inductor. 开关端口,连接外部功率电感。
EP	GND	Exposed pad of the device, also the ground of the device, connect it to a whole large copper plane on PCB for better thermal performance. 器件外露散热片,同时也是芯片地,连接至PCB大片铺铜,以增加散热。



SPECIFICATIONS

• Absolute Maximum Ratings ²

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
VIN supply voltage	VIN	-0.3		130	V
BST voltage	BST	-0.3		135.5	V
BST voltage (10ns transient)	BST	-0.3		137.5	V
Voltage between BST and SW	BST to SW	-0.3		5.5	V
FB voltage	FB	-0.3		5.5	V
RT voltage	RT	-0.3		5.5	V
PG voltage	PG	-0.3		14	V
EN voltage	EN	-0.3		130	V
SW voltage	SW	-1.5		130	V
SW voltage (10ns transient)	SW	-3		132	V
Moisture Sensitivity Level (MSL)			MSL3		
Junction Temperature	TJ	-40		150	°C
Storage Temperature	Tstg	-55		150	°C
ESD, Human-body model (HBM)	HBM		±2000		V
ESD, Charged-device model (CDM)	CDM		\pm 500		V

• Recommended Operating Conditions

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
VIN supply voltage	VIN		5		120	V
BST voltage	BST		-0.1		125	V
Voltage between BST and SW	BST to SW		-0.1		5.5	V
FB voltage	FB		-0.1		4.5	V
EN voltage	EN		-0.1		VIN	V
SW voltage	SW		-1.8		120	V
Output current range	Іоит	Continuous		0.7		A
Junction Temperature	TJ		-40		125	°C

• Electrical Characteristics

VIN = 24V, T_A = +25°C, unless otherwise noted.

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
		Rising		5		V
VIN UVLO threshold	Vuvlo	Falling		4.6		V
VIN UVLO hysteresis	V _{hys}			0.4		V
		V _{EN} = 1.25V, Standby mode, no switching		17		uA
Quiescent supply current	l la	V _{EN} = 2.5V, FPWM		500		uA
		V _{EN} = 2.5V, PFM		10		uA
Shutdown supply current	Isd	V _{EN} = 0V		3		μA
High-side switch on resistance	RDS(ON)_H			1800		mΩ
Low-side switch on resistance	RDS(ON)_L			700		mΩ
High-side peak current limit	IHS_PK_OC			0.84		A
Low-side peak current limit	ILS_PK_OC			0.84		A
Min of I _{HS_PK_OC} or I _{LS_PK_OC} minus I _{LS_V_OC}	ΙΔΟΟ			0.168		A
Low-side negative current limit	I _{LS_NOC}			1.5		A
Low-side valley current limit	ILS_VOC			0.672		A
Hiccup time before re-start	Tw			64		ms

¹ Depending on parts and PCB layout, characteristics may be changed.

² Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability



HTN77A0 Buck Converter

	VENR	EN rising, enable switching		1.5		V
	V _{ENF}	EN falling, disable switching		1.4		V
EN threshold	VLDOR	EN rising, enable LDO mode, no switching			1.1	V
Power-good threshold Power-good on-resistance Feedback voltage FB input current Minimum on time Minimum off pulse width	VLDOF	EN falling, disable LDO mode	0.45			V
Power-good threshold	Vfb_pgf	FB falling, PG high to low		1.08		V
	V_{FB_PGR}	FB rising, PG low to high		1.14		V
Power-good on-resistance	R _{PG}			7		Ω
Feedback voltage	VFB			1.2		V
FB input current	I _{FB}	V _{FB} = 1.2V	-100		100	nA
Minimum on time	t _{ON_MIN}			50		ns
Minimum off pulse width	toff_min			50		ns
Soft-start time	tss			3		ms
	4		100		1000	kHz
Switching frequency range	f _{sw}	RT = 24.9KΩ, VOUT = 5V		500		kHz
		Trigger thermal shutdown		160		°C
Power-good threshold Power-good on-resistance Feedback voltage FB input current Minimum on time Minimum off pulse width		Hysteresis		25		°C



1 Enable Control (EN pin)

The HTN77A0 is enabled when the VIN pin voltage rises above 5V and the EN pin voltage exceeds the enable threshold 1.5V (typical).

When the voltage of EN pin is between 1.1V and 1.3V (typical), the device is in Standby mode.

The HTN78A3 is disabled when the VIN pin voltage falls below 4.6V or when the EN pin voltage is low (below 0.45V typical).

2 Switching Frequency Setting (RT pin)

The switching frequency of the device in PWM mode is set by the RT resistor, use the formula below-

当 VIN 高于 5V 且 EN 高于 1.5V(典型值) 时,HTN77A0正常工作。

当 VIN 电压高于 5 V 且 EN 引脚电压在 1.1V~1.3V 之间(典型值), HTN77A0 工作于 Standby 模式。

当 VIN 引脚的电压降至 4.6 V 以下或 EN 引 脚的电压低于阈值(0.45V 典型值)时, HTN77A0 关断。

HT77A0 的开关频率(PWM 模式时)由电阻 RT 设置,参考如下公式。

$$f_{SW}(kHz) = \frac{2500 \times V_{OUT}(V)}{R_T(k\Omega)}$$
(5)

3 Working mode (HTN77A0F vs HTN77A0P)

The HTN77A0F works in FPWM mode at light loads and heavy loads, while HTN77A0P works in PWM mode at heavy loads and automatically transitions into PFM mode for high efficiency.

4 Output voltage Setting (FB pin)

The output voltage of the device is set by the Rp and Rd resistor (shown as in the typical application), use the formula below-

$$V_{OUT}(V) = 1.2 \times (1 + \frac{R_P}{R_D})$$

5 Power Good (PG pin)

The PG pin of the device can indicate whether the output voltage is within the regulation level. It could be used as a power good flag to monitor the output and act a startup sequencing or fault protection design if necessary.

The PG pin is an open-drain output that requires a pullup resistor $(10k\Omega \sim 100k\Omega)$ to a DC supply lower than 14 V.

When the FB voltage exceeds 95% of the internal reference VREF, the PG pin is in High-Z and it can be pulled high by the external pullup resistor.

If the FB voltage falls below 90% of VREF, an internal 7Ω switch pulls the PG low to indicate that the output voltage is out of regulation. The rising edge of PG has a built-in deglitch delay of 5 µs.

HTN77A0F 在轻载和重载时都工作在强制 PWM 模式,而 HTN77A0P 在重载时工作在 PWM 模式,在轻载时工作在 PFM 模式以维持 高效率。

HT77A0 的输出电压通过 Rp 和 Rd 电阻设 置(如典型应用图),参考如下公式。

$$_{T}(V) = 1.2 \times (1 + \frac{R_{P}}{R_{D}})$$
 (5)

HTN77A0 提供 PG 标志引脚,以指示输出 电压何时在调节水平内。使用 PG 信号对下游转 换器进行启动排序或进行故障保护和输出监测。

PG 是一种开漏输出,需要一个上拉电阻连 接到不大于 14 V 的直流电源。上拉电阻的典型 范围为 10 k Ω 至 100k Ω 。如有必要,使用分压 器从更高电压的上拉轨降低电压。

当 FB 电压超过内部参考 VREF 的 95%时, PG 为高阻。PG 可通过外部上拉电阻拉高,表 示器件输出正常。

如果 FB 电压降至 VREF 的 90%以下,则 内部开关打开, PG 被拉低, 表示输出电压不稳 定。PG 的上升沿具有 5µs 的内置延迟。



6 Internal Linear Regulator and Bootstrap Voltage Regulator (BST pin)

An internal linear regulator powered from VIN with a nominal output of 5 V is integrated in the device, supplies current to internal circuit blocks. The input pin (VIN) can be connected directly to line voltages up to 130 V.

The power MOSFET driver is powered by an external bootstrap capacitor (C_{BOOT} at BST pin), which is recommended to use a 2.2nF capacitor. This floating driver has its own undervoltage lockout (UVLO) protection. The UVLO rising threshold is 2.9V with a hysteresis of 200mV. The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator-

7 Input Capacitor (VIN pin, C_{IN})

Bypass the VIN pin to GND with a low-ESR, high voltage ceramic capacitor. Make sure that the rating voltage of the capacitor is higher than the max input voltage. The capacitors should be placed as close to the VIN pin and GND pin as possible.

8 Output Inductor (SW pin)

The inductor peak-to-peak ripple current I_{L_PP} , peak current I_{L_PK} and RMS current I_{L_RMS} are calculated as following. The inductor saturation current rating must be greater than the I_{L_PK} and the RMS or heating current rating must be greater than I_{L_RMS} . Place the inductor as close to the SW pin as possible-

HTN77A0 包含一个内部线性稳压器,该稳 压器由 VIN 供电,输出为 5V,消除了对外部电 容器来稳定线性调节器的需要。内部 VCC 调节 器为内部电路提供电流。输入引脚(VIN)可以 直接连接到高达 130V 的线电压。

功率 MOSFET 驱动由外部自举电容器 (BST 端的 C_{BOOT} 电容)供电,其建议使用一 个 2.2nF 的陶瓷电容。该功率管有其自身的欠压 锁定(UVLO)保护。UVLO 上升阈值为 2.9V, 磁滞 200mV。内部自举调节器通过外部自举电 容充电调节至约 5V。

VIN 端和 GND 端应放置低 ESR 的滤波陶 瓷电容,确保电容的额定电压高于最大输入电压。电容应尽可能靠近 VIN pin 和 GND pin 放置。

电感峰峰值电流 IL_PP、峰值电流 IL_PK 和 RMS 电流 IL_RMS 计算如下。电感额定饱和电流 必须大于 IL_PK, RMS 或热电流额定值必须大于 IL_RMS。电感需尽量靠近 SW 引脚放置。

$$I_{L_{PP}} = \frac{V_{OUT}}{V_{IN_{MAX}}} \times \frac{V_{IN_{MAX}} - V_{OUT}}{L \times f_{SW}}$$
(3)

$$I_{L_{PK}} = I_{OUT} + \frac{I_{L_{PP}}}{2} \tag{4}$$

$$I_{L_{RMS}} = \sqrt{I_{OUT}^{2} + \frac{1}{12} \times I_{L_{PP}}^{2}}$$
(5)

9 Output Capacitor (C_{OUT})

The output capacitor limits the voltage ripple. Use 输出电容可以减小输出纹波,输出电容应大 capacitors larger than: 于:

 $C_{OUT} > \frac{I_{L_{PP}}}{8 \times f_{SW} \times V_{ripple}}$ (5)

10 Soft Start

The HTN77A0 employs an internal 3ms soft start to ramp up the FB voltage from 0V to 1.2V linearly once EN pulled high. HTN77A0 采用内部 3ms 软启动,一旦 EN 拉高,FB 电压就会线性上升至 1.2V。



11 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at an insufficient supply voltage. The UVLO rising threshold is about 5V, while its falling threshold is about 4.6V.

12 Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than its upper threshold, the entire chip shuts down. When the temperature is lower than its lower threshold, the chip is enabled again.

13 PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to following figure and follow the guidelines below.

(1) Place the input capacitor and output capacitor as close to the device as possible.

(2) Keep the power traces very short and fairly wide, especially for the SW node.

This can help greatly reduce voltage spikes on the SW node and lower the EMI noise level.

(3) Run the feedback trace as far from the inductor and noisy power traces (like the SW node) as possible.

欠压锁定(UVLO)功能可避免芯片工作在 电源电压不足的条件。UVLO上升阈值约为5V, 下降阈值为4.6V。

过热关断保护是为了防止芯片在极高的温 度下工作。当芯片温度高于其上限阈值时,整个 芯片关闭。当温度低于其下限阈值时,芯片再次 启用。

有效的 PCB 布局对于稳定运行至关重要。 要获得最佳结果,请参考下图并遵循以下指南。

(1)将输入电容、输出电容尽可能靠近芯 片。

(2)保持电源轨迹非常短且相当宽,特别 是对于 SW 节点。

这有助于大大降低 SW 节点上的电压尖峰, 并降低 EMI 噪声水平。

(3) FB 走线尽可能远离电感和功率走线 (如 SW 节点)。



PACKAGE OUTLINE

ESOP8







D	Dimension millimeters							
字符	Min	Standard	Max					
A	1.350	1.500	1.700 0.100 1.550 0.440					
A1	0	0.050						
A2	1.350	1.450						
b	0.360	0.400						
С	0.215	0.220	0.235					
D	4.800	4.900	5.000 4.040					
E	3.840	3.940						
E1 5.900		6.000	6.100					
е	1.27BSC							
L	0.400	0.550	0.700					
Θ	0 °		8 °					





■ TAPE AND REEL INFORMATION





A0	ormonont width, 划槽空座					
	component width; 料槽宽度					
BO	Dimension designed to accommodate the					
BU	component length;料槽长度					
ко	Dimension designed to accommodate the					
KU	component thickness; 料槽厚度					
W	Overall width of the carrier tape;					
vv	载带整体宽度					
D1	Pitch between successive cavity centers;					
P1	相邻槽中心间距					

编带 PIN1 方位象限分配 Quadrant Assignments for Pin1 Orientation in Tape

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器件料号 Part No.	封装 类型 Package Type	封装 标识 Package Abbr.	引脚 数 Pins	SPQ	料盘 直径 D _R (mm)	料盘 宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 象限 Quadrant
HTN78A3SPER	ESOP	SPE	8	2500	330	12	6.55	5.55	1.95	8	12	Q1



■ TAPE AND REEL BOX INFORMATION



器件料号 Part No.	封装类型 Package Type	封装标识 Package Abbr.		SPQ	长度 Length (mm)	宽度 Width (mm)	高度 Height (mm)
HT78A3SPER	ESOP	SPE	8	5000	360	345	65



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