1 Description

SS1311 是一款性能与功耗卓越、性价比极高的单声道音频编解码芯片。该芯片集成了信噪比高达 106dB 的 ADC 和 110dB 的 DAC，可满足高性能音频的应用需求。同时，它具有领先的低功耗水平，适合便携式、智能化、工业等广泛的应用。SS1311 集成了低噪声 ALDO/DLDO，支持单电源供电，具备高性能抗混叠能力、工业/车规级 ESD，方便实现简洁、可靠的方案。此外，它包含 0 至 42dB 模拟 PGA、AB 类耳机放大器，I2S 接口、数字麦克风接口、数字音量，以及先进的片上信号处理单元，包括可编程均衡器（EQ）、动态范围压缩器（DRC）、HPF、音量淡入淡出等功能。它还内置了一个锁相环（PLL），支持各种输入时钟，适应灵活、精准的频率应用要求。

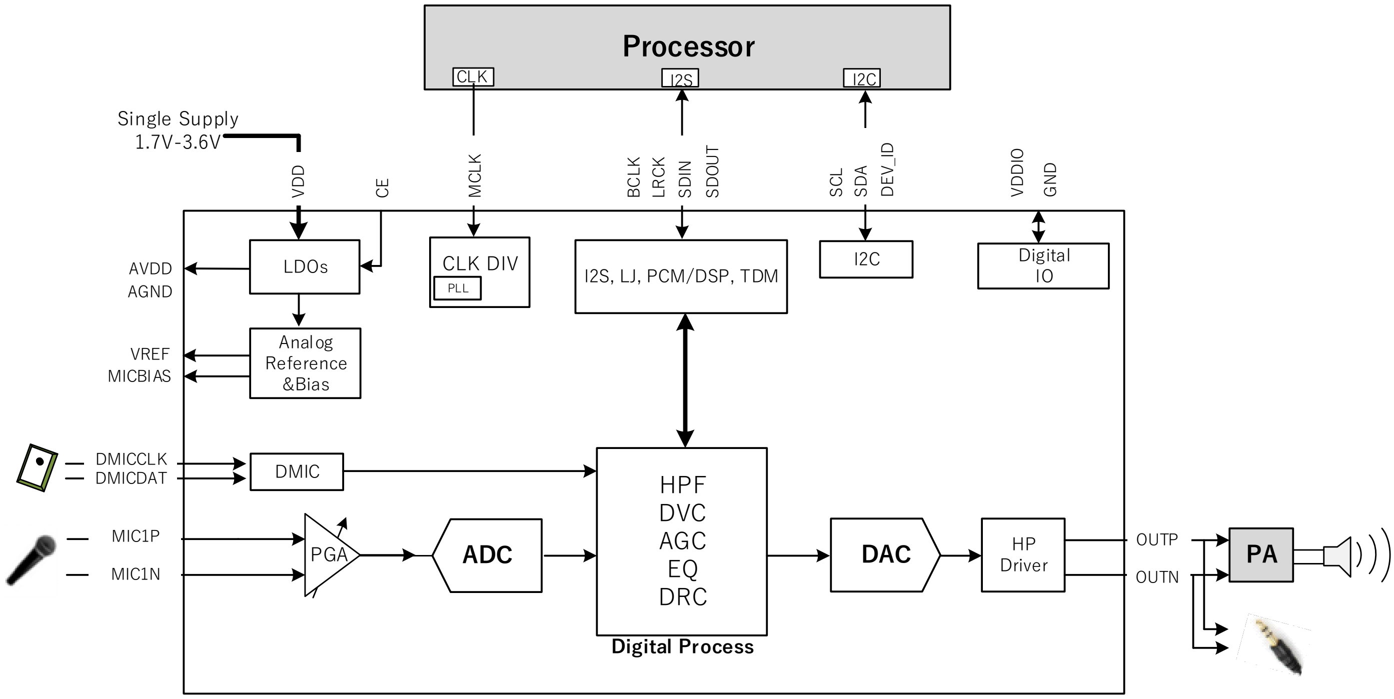
2 FEATURES

- Mono ADC Channel
  - Performance:
    - SNR: 106 dB
    - THD+N: –92 dB
  - Sample Rate (fs) = 8 KHz to 192 KHz
  - Programmable PGA Gain from 0dB to 42dB
- Mono DAC Channel
  - Performance:
    - SNR: 110 dB
    - THD+N: –96 dB
  - Sample Rates (fs) = 8 KHz to 192 KHz
- Digital Process
  - Programmable IIR Filters for Noise Reduction
  - HPF for ADC DC Remove
  - 3 Band EQ
  - Dynamic Range Compressor (DRC)
  - Soft Volume Control/ Soft Mute
- Analog Input/Output
  - 1 Differential MIC Input
  - 1 Low Noise MIC Bias Output
    - from 1.8V to 2.5V
    - 3.3 uVrms Noise between 20Hz-20KHz
  - 1 Differential Line-out Output
    - Support Single Mode
    - Can Used as a Headphone Driver (9mW@ 32Ω) without Pop Noise
- Power
  - Single Supply Operation: 1.8 V- 3.3 V
    - Integrated Low Noise ALDO and DLDO
  - Low-Power Consumption
    - 5mW for Playback and Record
- Digital Interface
  - I2C Control Interface
  - I2S Audio Data Serial Interface
- Flexible Features
  - Programmable PLL for Flexible Clocking
  - Digital Microphone Input Support
- Package
  - 3mm×3mm 20-Pin QFN

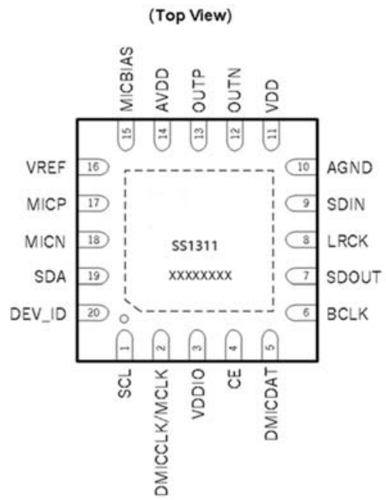
3 APPLICATIONS

- Music Player/Recorder
- IPC, DVR, NVR
- Dash Cam
- Phone
- Toy
- Portable Devices

4 BLOCK DIAGRAM



5 Pin Configuration and Functions



PIN Functions

PIN	NAME	TYPE①	DESCRIPTION
1	SCL	DI	I2C interface serial clock input (Open-drain)
2	MCLK DMICCLK	DIO	Master clock input Digital MIC clock output
3	VDDIO	Power	Digital power for digital I/O
4	CE	DI	Chip enable pin (active HIGH)
5	DMICDAT	DI	Digital MIC serial data input
6	BCLK	DIO	I2S interface bit clock
7	SDOUT	DO	I2S interface serial data output
8	LRCK	DIO	I2S interface word clock
9	SDIN	DI	I2S interface serial data input
10	AGND	Ground	Analog Ground
11	VDD	Power	Chip voltage supply, 1.8V-3.3V
12	OUTN	AO	Analog negative differential output from DAC
13	OUTP	AO	Analog positive differential output from DAC
14	AVDD	Power	Analog LDO output
15	MICBIAS	AO	AMIC bias voltage output
16	VREF	AO	Analog reference
17	MICP	AI	Analog positive differential input for ADC
18	MICN	AI	Analog negative differential input for ADC
19	SDA	DIO	I2C interface serial clock input (Open-drain)
20	DEV_ID	DI	LSB of I2C bus address control
EPAD	GND	Ground	Chip Ground

① DI (Digital Input), DO (Digital Output), DIO (Digital Input/Output), AI (Analog Input), AO (Analog Output), AIO (Analog Input/Output)

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Supply voltage range	VDD	-0.3	3.6	V
	VDDIO	-0.3	3.6	V
	AVDD①	-0.3	2.2	V
Digital input voltage to DGND		-0.3	VDDIO + 0.3	V
Analog input voltage to AGND		-0.3	AVDD + 0.3	V
Operating temperature, T_A		-40	85	℃
Junction temperature, (T_J Max)			125	℃
Storage temperature, T_{stg}		-65	150	℃

① Normally, it is powered by an internally integrated LDO

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Human body model(HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±8000	V
	Charged device model(CDM), per ANSI/ESDA/JEDEC JS-002, , all pins	±500	

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
VDD	Supply voltage range for ALDO and DLDO	1.7①	3.3	3.6	V
VDDIO	Supply voltage range for Digital I/O	1.6	3.3	3.6	V
AVDD	Supply voltage range for Analog circuits	1.7	1.8	2.0	V
MCLK	Master clock frequency			25	MHz
SCLK	SCL clock frequency			400	KHz
	PLL input frequency	0.512		20	MHz

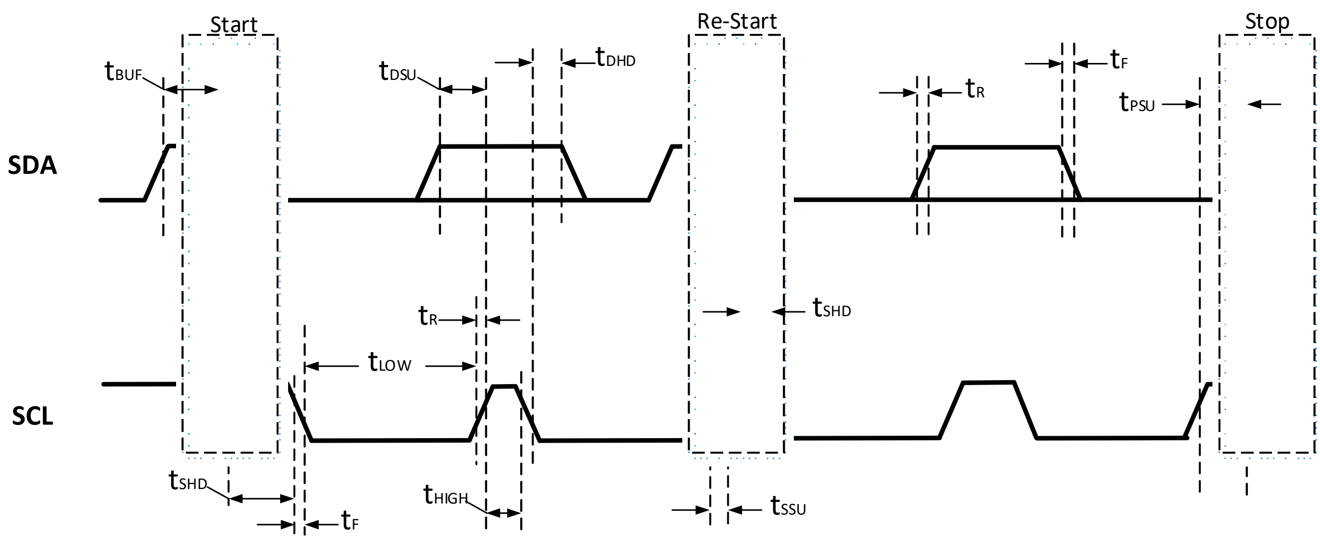
① When VDD cannot guarantee the minimum value of 1.7V or above, please short VDD and AVDD together on the PCB.

6.4 Digital IO specifications

6.4.1 Digital IO DC Characteristics

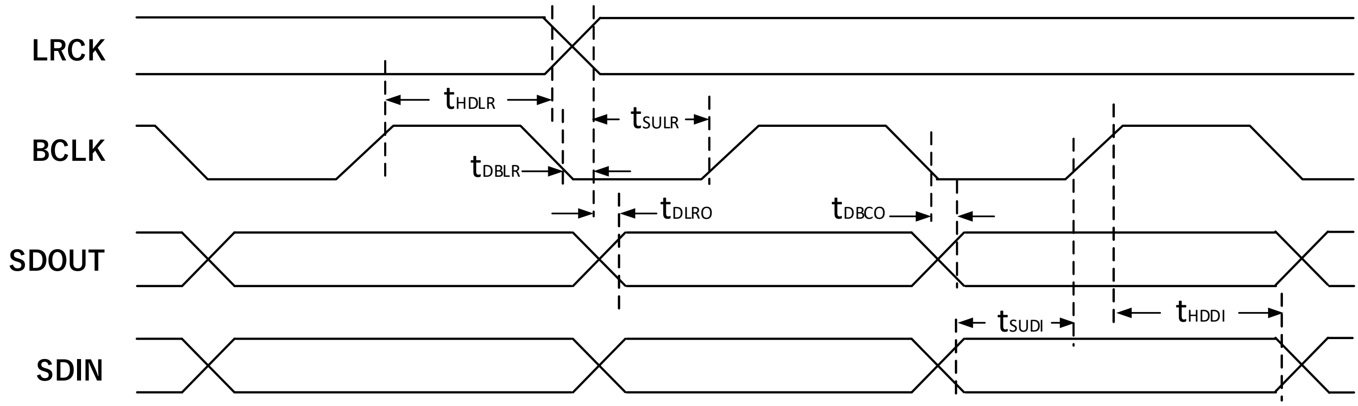
		Conditions		MIN	MAX	UNIT
V_{IH}	High level input	VDDIO=3.3V		0.51*VDDIO		
		VDDIO=1.8V		0.53*VDDIO		V
VIL	Low level input	VDDIO=3.3V			0.42*VDDIO	
		VDDIO=1.8V			0.41*VDDIO	V
V_{OH}	High level output	I_{load}=1mA	VDDIO=3.3V	0.98*VDDIO		
		Driven= 0	VDDIO=1.8V	0.93*VDDIO		V
V_{OL}	Low level output	I_{load}=1mA	VDDIO=3.3V		0.02*VDDIO	
		Driven= 0	VDDIO=1.8V		0.07*VDDIO	V
C_{OUT}	Digital output load capacitance				10	pF

6.4.2 I2C Timing Characteristics



		MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	0	-	400	kHz
t_{LOW}	LOW period of the SCL clock	1.3	-		us
t_{HIGH}	HIGH period of the SCL clock	0.6	-		us
t_{SSU}	Set-up time for a repeated START condition	0.6	-		us
t_{SHD}	Hold time for a (repeated) START condition.	0.6	-		us
t_{DSU}	Data Hold time	0	-	0.9	us
t_{DHD}	Data Set-up time	100	-		us
t_R	SDA and SCL Rise Time		-	0.3	us
t_F	SDA and SCL Fall Time		-	0.3	us
t_{PSU}	Set-up time for STOP condition	0.6	-		us
t_{BUF}	Bus free time between a STOP and START condition	1.3	-		us

6.4.3 I2S Timing Characteristics



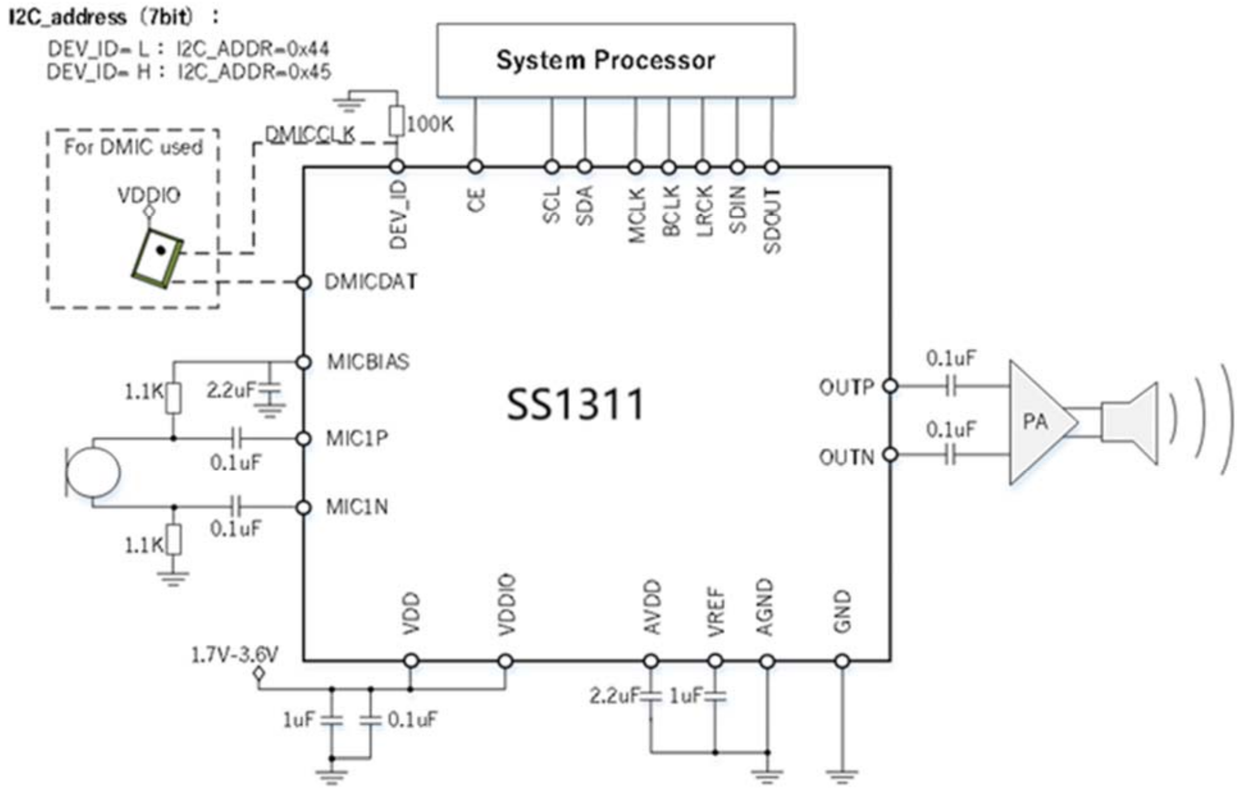
		MIN	TYP	MAX	UNIT
f_{MCLK}	MCLK clock frequency		-	25	MHz
f_{BCLK}	BCLK clock frequency		-	20	MHz
f_{LRCK}	LRCK clock frequency		-	200	kHz
t_{DBLR}	BCLK to LRCK delay (For Master mode only)			20	ns
t_{HDLR}	LRCK Hold time (For Slave mode only)	10			ns
t_{SULR}	LRCK Set-up time (For Slave mode only)	10			ns
t_{DOLR}	SDOUT to LRCK delay		-	20	ns
t_{DOBC}	SDOUT to BCLK delay		-	20	ns
t_{SUDI}	SDIN Set-up time	10			ns
t_{HDDI}	SDIN Hold time	10			ns

6.5 Typical Performance Characteristics

At 25°C, VDD=3.3V, VDDIO= 3.3 V, fs = 48KHz, 1kHz sine wave input unless otherwise specified

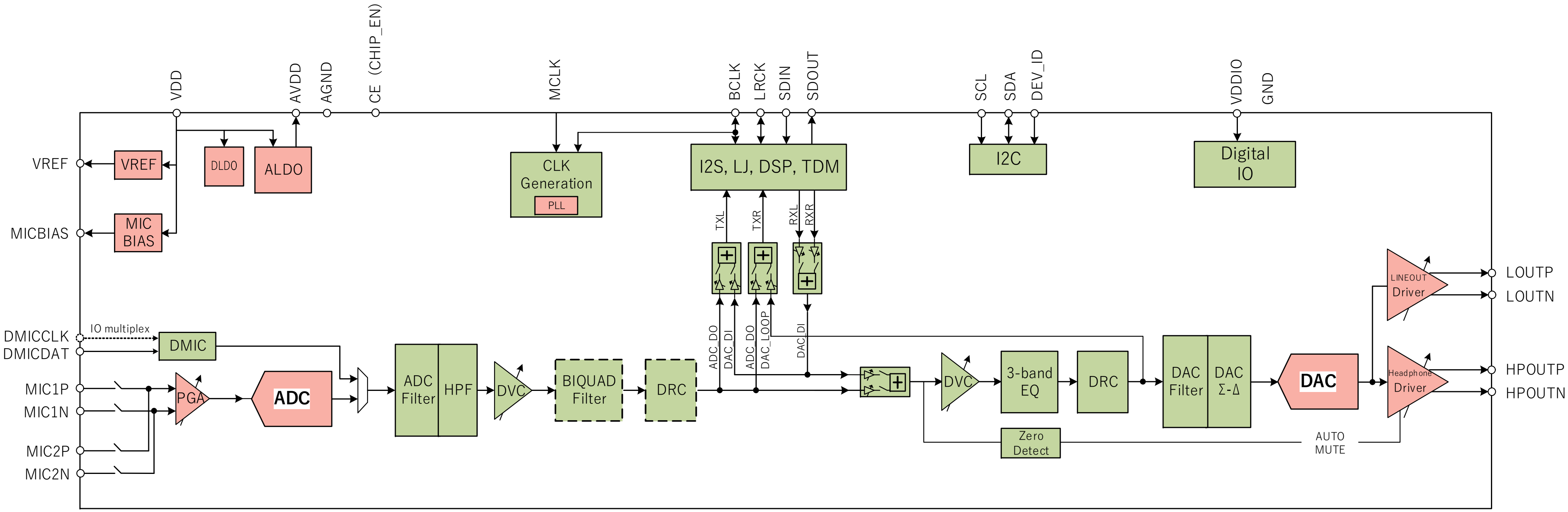
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
AUDIO ADC						
VIN_{max}	Full Scale Input Level	Differential input		1.4		V_{RMS}
SNR	Signal-to-Noise Ratio (A-weight)	PGA gain = 0 dB		106		dB
		PGA gain = 12 dB		102		dB
		PGA gain = 30 dB		91		dB
THD+N	Total Harmonic Distortion and Noise	PGA gain = 0 dB		-92		dB
		PGA gain = 12 dB		-90		dB
		PGA gain = 30 dB		-83		dB
Freq. Response	Filter gain from 0 to 0.42 fs			±0.05		dB
	Filter gain from 0.55 fs to 64 fs			-70		dB
	PGA gain range	gain step = 3dB	0		42	dB
R_{IN}	Input Resistance		12.5	100	400	KΩ
MICBIAS						
	Bias voltage		1.8	2.1	2.5	V
	Current sourcing			2		mA
	Integrated noise	BW = 20 Hz to 20 kHz, A-weight		3.3		uV_{RMS}
AUDIO DAC						
$VOUT_{max}$	Full Scale Output Level	Differential output		1.25		V_{RMS}
SNR	Signal-to-Noise Ratio (A-weight)	Auto-mute function enabled		114		dB
	Signal-to-Noise Ratio (A-weight)	Auto-mute function disabled		110		dB
THD+N	Total Harmonic Distortion and Noise			-96		dB
Freq. Response	Filter gain from 0 to 0.42 fs			±0.05		dB
	Filter gain from 0.55 fs to 64 fs			-70		dB
P_O	Output Power	R_L=32Ω@single mode		9		mW
POWER CONSUMPTION @ fs = 48 kHz						
Power down		CE pin pull low, Pad disable		0		uA
PLL		Additional power consumed when PLL is powered for Non-standard clock input		0.5		mA
Mono record + Mono play		PLL off, MCLK=6.144M, PGA =42dB, silence		2.8		mA

7 Typical Application



8 Detailed Descriptions

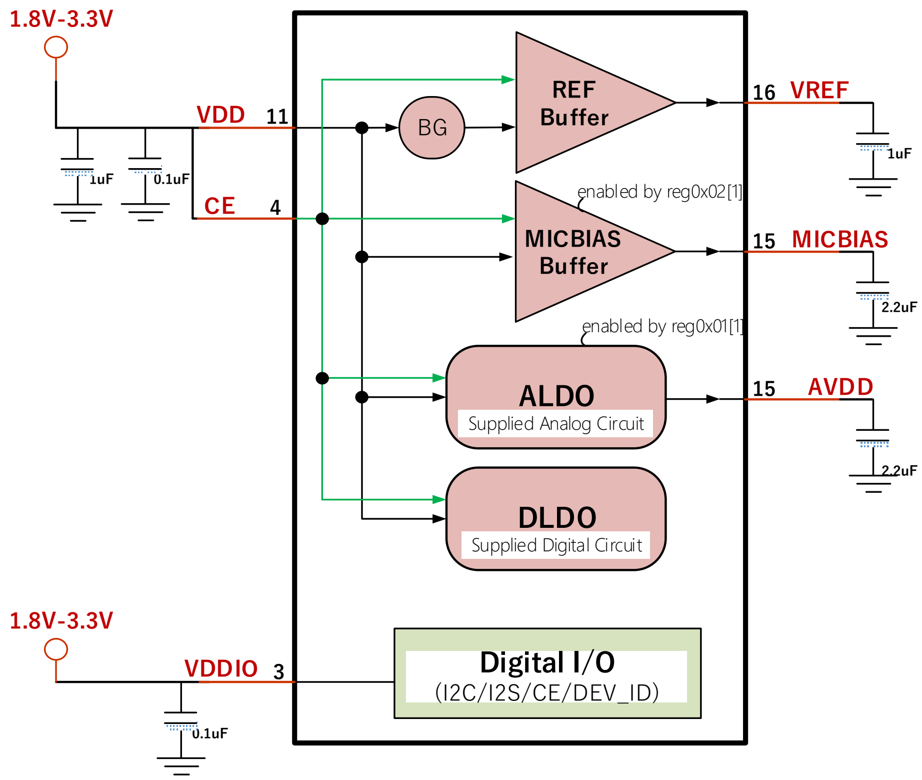
8.1 Functional Block Diagram



FUNCTION BLOCK DIAGRAM

8.2 Power

The SS1311 only requires a single power supply, a 3.3V nominal supply rail or a 1.8V nominal supply rail for VDD and VDDIO to freely choose from, making it easy to be used in various scenarios.



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VDD is a common power input for built-in ALDO and DLDO, and VDD input range is 1.7V to 3.3V. The ALDO output pin AVDD with an external 2.2uF decoupling capacitor, which is designed to supply analog circuit operated from 1.6-V to 2.0-V. DLDO is a capless LDO to supply digital circuit. VREF is designed to be a low noise voltage as analog power reference. VDDIO is digital I/O power to operate from1.6V to 3.6V for I2C, I2S, CE, and DEV_ID. The built-in LDO and clean reference make sure analog circuit work in a high-performance status even in highly noise-sensitive circuits.

When the CE pin remains low, all LDOs will be turned off and the logic circuit will be in a reset state. At this time, the leakage current is<0.01uA. When the CE pin goes high, VREF and DLDO will automatically activate. VREF outputs 1/2 AVDD voltage. AVDD and MICBIAS voltages are enabled by Reg_0x01 and Reg_0x02.

8.3 Reset

There are 2 types of reset operation: power on reset (POR) and register reset.

The POR circuit in SS1311 used to reset all the circuit and register to a standby state after power up. The POR circuit make the VDD and VDDIO supply need no specific timing.

A software reset can be asserted by I2C set Reg_0x00 from 0 to 1. This bit make all the register and the corresponding circuit reset to the default state except I2C itself.

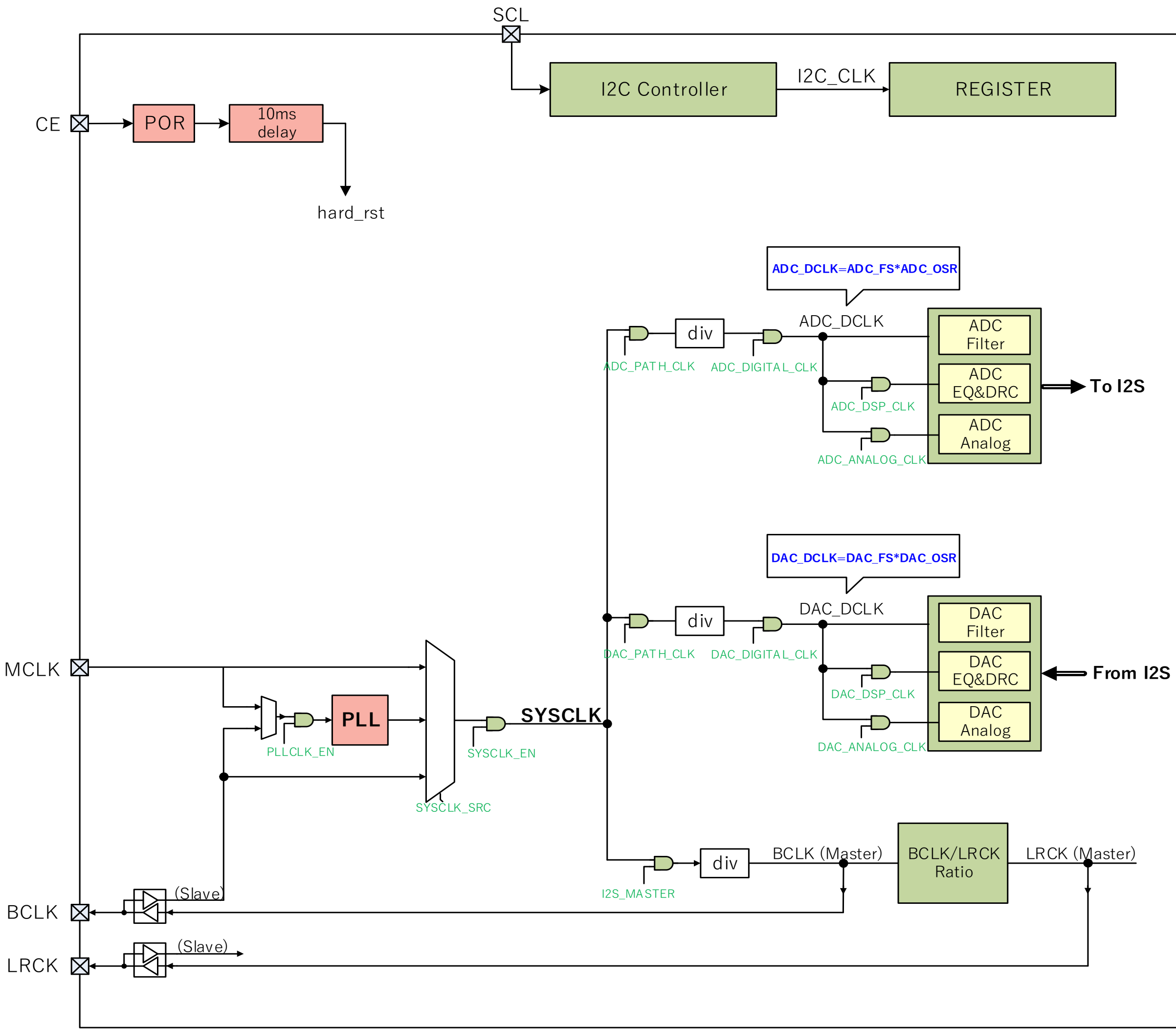
8.4 Clock

The SS1311 needs an external clock source to generate the system clock (SYSCLK). SYSCLK can be selected from MCLK, BCLK or PLL. MCLK is always provided externally while the reference clock of PLL can be selected from MCLK or BCLK. The driver should arrange the clock of each block and setup each divider.

As shown in the diagram below, the SYSCLK needs to be divided to generate ADC block clock, DAC block clock, and I2S block clock. The ADC block clock needs to be equal to ADC_OSR x ADC_FS, and the DAC block clock needs to be equal to DAC_OSR x DAC_FS. The standard audio frequencies of sampling (FS) from 8 kHz to 192 kHz are supported. These dividers are set by Reg_0x0C, Reg_0x0D, and Reg_0x0E.

The I2S of SS1311 can work in either master or slave mode. When in slave mode, BCLK and LRCK come from external pins, and no need to set up the clock divider. When in master mode, BCLK and LRCK are output pin, the clock is generated by SYSCLK divider through Reg_0x11 and Reg_0x12.

The I2C of SS1311 can only work in slave mode and the clock domain is independent. As long as POR is completed, register read and write can be performed without providing a system clock



Audio Clock Tree

8.5 PLL

A Phase-Locked Loop (PLL) is designed to cover a flexible input clock range from 512 KHz to 24 MHz. The clock sources of the PLL can be selected from MCLK or BCLK by setting register. The PLL output is always used to provide the system clock (SYSCLK) for the SS1311 chip when the ADC_DCLK or DAC_DCLK cannot be divided from MCLK or BCLK.

The PLL supports standard audio clocks (64Fs, 128Fs, 256Fs, 384Fs, 512Fs, etc.), USB clocks (12/24 MHz), and some other common non-standard audio clocks (13 MHz, 15.36MHz, 19.2 MHz, 19.68MHz etc.).

The PLL transmit formula as below:

$$FOUT = FIN * N / (M*P)$$

Table1. Clock Setting Table for 48 kHz series (Unit: MHz)

	FIN	N	P	FVCO	M	FOUT
Standard clock	0.512	192	1	98.304	16	6.144
	0.768	128	1	98.304	16	6.144
	1.024	96	1	98.304	16	6.144
	1.536	64	1	98.304	16	6.144
	2.048	96	2	98.304	16	6.144
	3.072	96	3	98.304	16	6.144
	4.096	96	4	98.304	16	6.144
	4.608	64	3	98.304	16	6.144
Non-standard clock	6	82	5	98.4	16	6.15
	12	82	10	98.4	16	6.15
	13	68	9	98.22222	16	6.139
	15.36	64	10	98.304	16	6.144
	16	92	15	98.13333	16	6.133
	19.2	82	16	98.4	16	6.15
	19.68	95	19	98.4	16	6.15

Table2. Clock Setting Table for 44.1 kHz series (Unit: MHz)

	FIN	N	P	FVCO	M	FOUT
Standard clock	0.7056	128	1	90.3168	16	5.6448
	1.0584	96	1	101.6064	18	5.6448
	1.4112	64	1	90.3168	16	5.6448
	1.5876	64	1	101.6064	18	5.6448
	2.1168	96	2	101.6064	18	5.6448
	2.8224	96	3	90.3168	16	5.6448
	3.1752	64	2	101.6064	18	5.6448
	4.2336	96	4	101.6064	18	5.6448
Non-standard clock	6	113	6	113	20	5.65
	12	113	12	113	20	5.65
	13	113	13	113	20	5.65
	15.36	86	13	101.6123	18	5.6451
	16	113	16	113	20	5.65
	19.2	53	10	101.76	18	5.6533
	19.68	62	12	101.68	18	5.6489

8.6 I2C Interface

The SS1311 supports the I2C-compatible serial bus and the data transmission protocol for standard-mode and fast-mode (CB max = 100 pF) as a slave device. This protocol is explained in the well-known I2C 2.0 specification.

The SS1311 has 7 bits for its own slave address. The first six bits of the slave address are factory preset to 10 0010. The last 1-bit of the address byte is the device select bit, which can be user-defined by the DEV_ID pin.

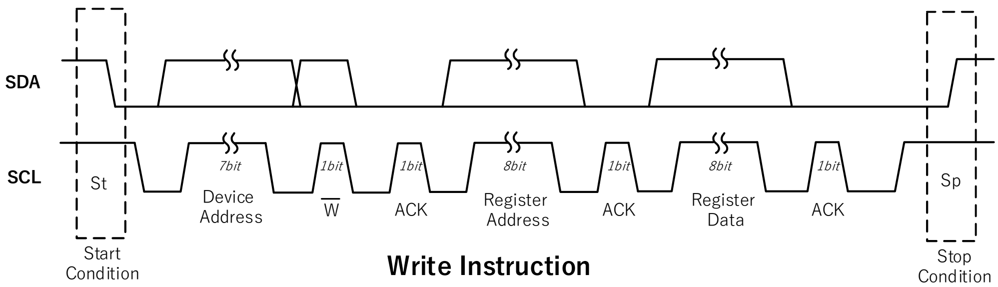
Slave Address

MSB							LSB
1	0	0	0	1	0	DEV_ID	R/$\overline{W}$

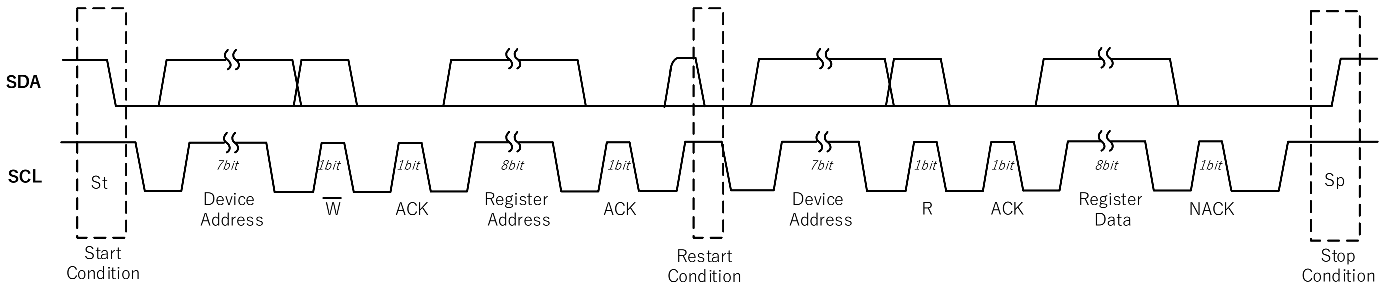
Packet Protocol

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCK is high. The first byte transferred is the slave 7-bit address followed by a R/W bit. The R/W bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the R/W bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCK is high.

The formats of “write” and “read” instructions are shown in below.



Write Instruction



Read Instruction

$\overline{W}$: 0 for Write Command R : 1 for Read Command

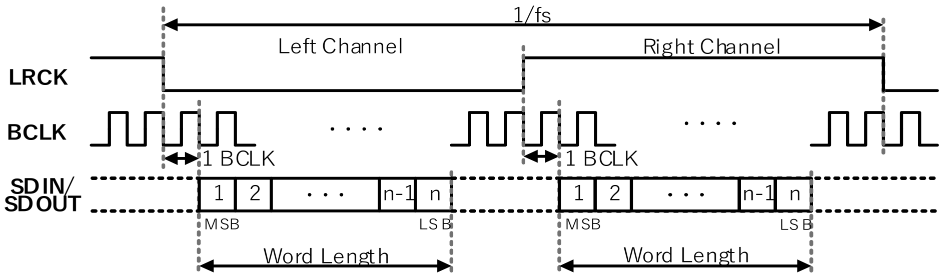
ACK : 0 , Slave-to-Master NACK : 1 , Master-to-Slave

8.7 I2S/PCM Interface

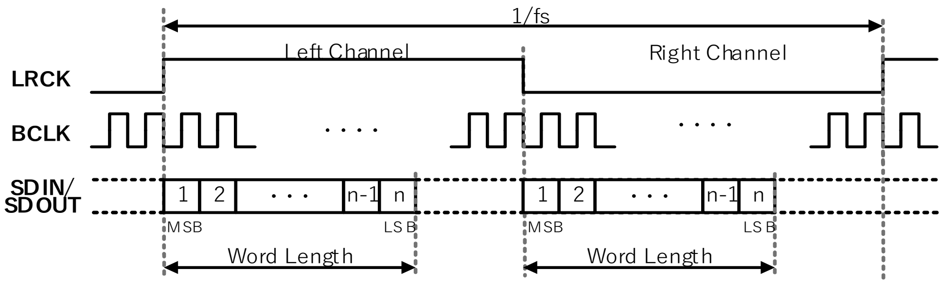
The SS1311 device audio serial port consists of 4 signals: BCLK, LRCK, SDOUT and SDIN. The audio interface supports slave mode and master mode. BCLK/LRCK are input at the slave mode and output at the master mode.

SS1311 audio interface support I2S standard mode, left justified mode and DSP/PCM mode as shown in the following figure.

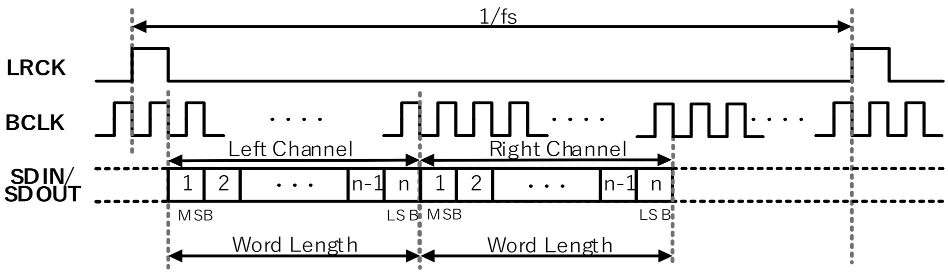
The 2-channel TDM mode is also supported, and two SS1311 can be combined up to drive the I2S bus, suitable for stereo playback or recording applications. The data driven on left-channel or right-channel can be freely selected from either chip.



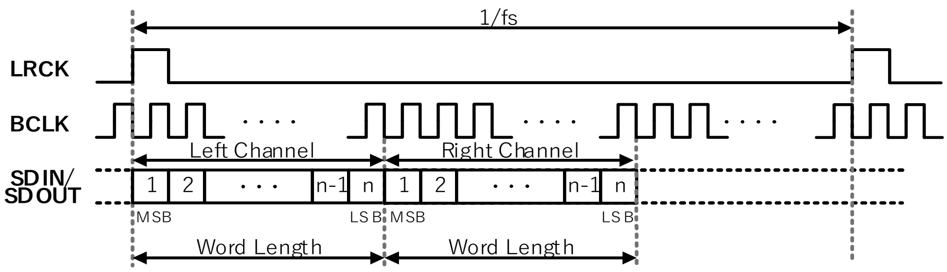
I2S standard mode (Offset=1)



Left Justified mode (Offset=0)



DSP_A mode (Offset=1)



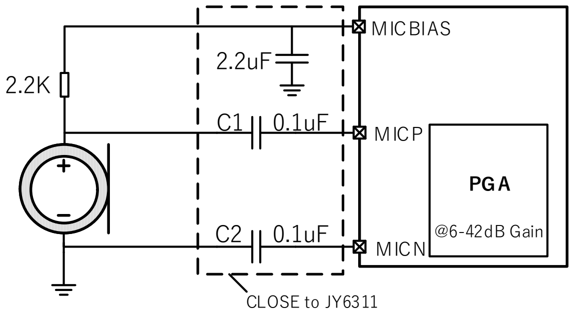
DSP_B mode (Offset=0)

8.8 Analog Input

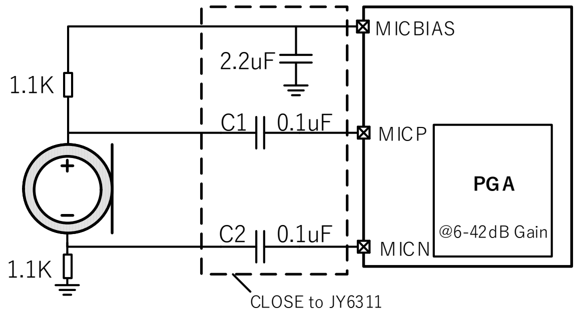
The analog input pins of SS1311 named MICP/N provide differential input signal to the PGA in ADC record path. The PGA is programmable from 0 dB to 42 dB, 3db per step, suitable for flexible inputs, such as various microphones or line-in inputs.

Usually, MICP/N must be AC-coupled to microphone or line-in signals. The AC-coupling capacitor causes a high-pass filter pole to be inserted into the analog signal path, so the size of the capacitor must be chosen to move that filter pole on optimal frequency to remove the unwanted DC and sufficiently low frequency. The cut-off frequency of the high-pass filter is Fc = 1/(2* π *Ri*Ci). When the PGA is 0dB, R is 16K, and when the PGA is in the range of 6 dB to 42 dB, R is 100K. For example, in a use of microphone, the PGA gain set to 42dB. The recommended capacitance value is C1=C2=0.1uF, and the Fc=1/(2*pi*100K*0.1uF) = 16Hz.

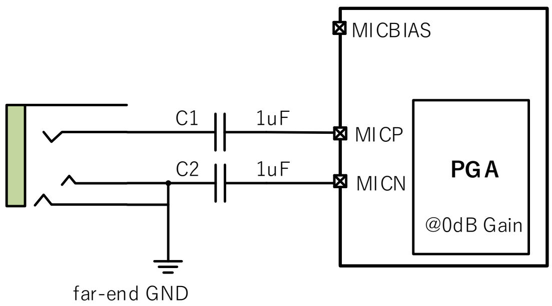
The device has a microphone bias output (MBIAS) with a 4mA maximum driving current, which is a programmable voltage source that can be used to supply microphone.



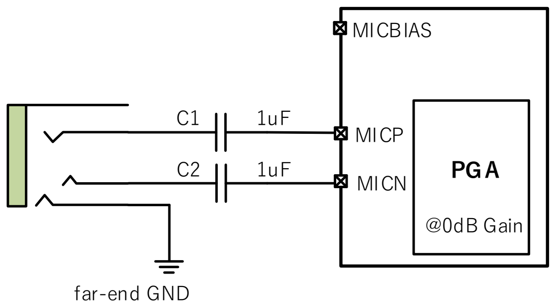
Single-Ended Mic Input



Differential Mic Input



Single-Ended Line-in



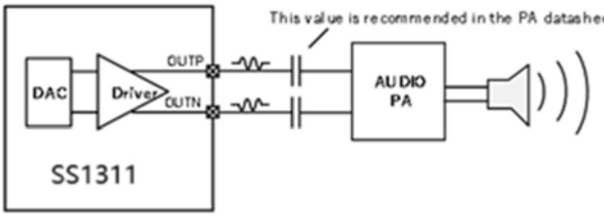
Differential Line-in

8.9 Analog Output

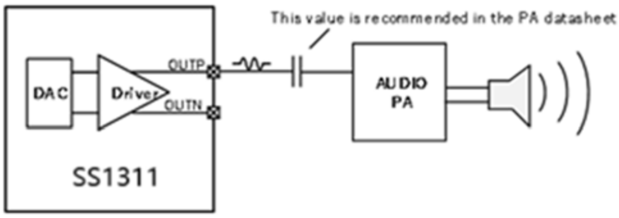
The analog output pins of SS1311 named OUTP/N provide differential line-out signal to the external audio PA driving the speaker in DAC play path. The pin OUTP can be set by register to a single-ended mode and can drive a maximum 9 mW load@32Ω. It is very useful in headphone applications.

The analog output operates at a common-mode voltage of AVDD/2. The common-mode voltage can result due to sudden transient changes in the output drivers if not prevented by careful design. SS1311 ramp up and ramp down the common-mode voltage gradually by using a slow power-up circuit controlled by Reg_0x81 to achieve pop-free effect. When this function is enabled, there must be a delay of at least some millisecond defined by DAC_RAMP_TIME before playing data in the audio stream.

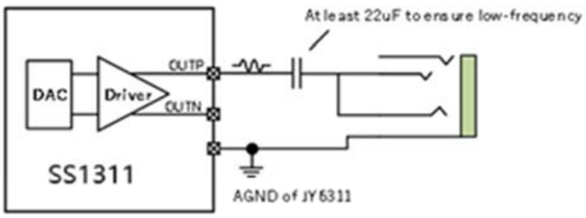
The recommended connection circuit is as follows.



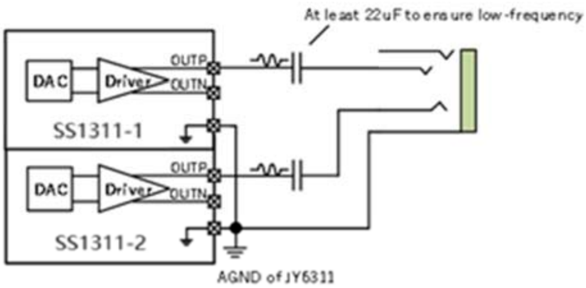
Line-out differential mode



Line-out single-ended mode



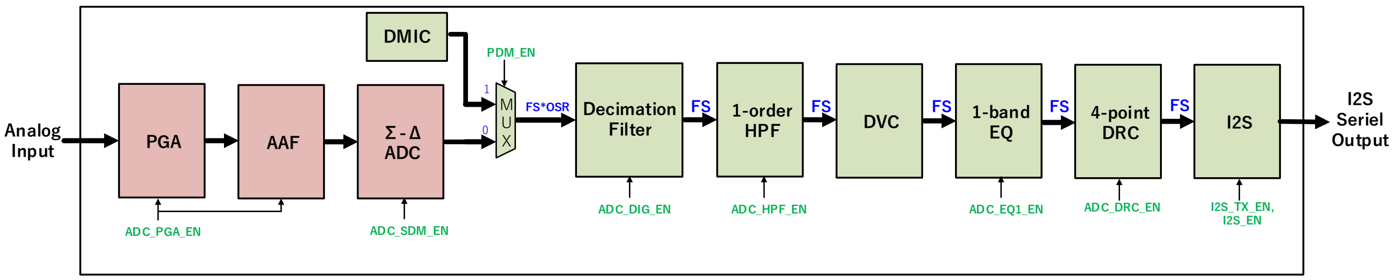
Headphone mono mode



Headphone stereo mode

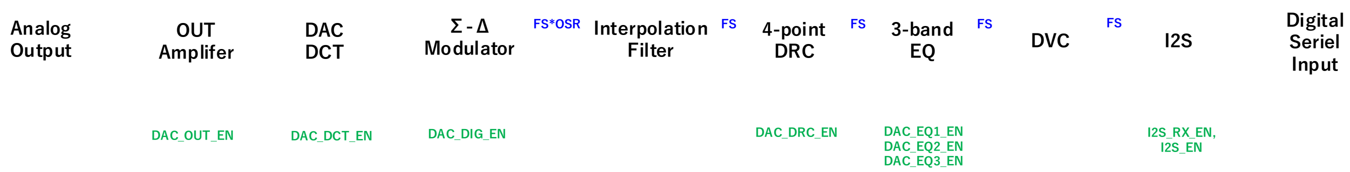
8.10 ADC

The ADC path includes a gain amplifiers (PGA) with a range of 0 to +42dB, an anti-aliasing filter (AAF) and a mono audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter and a digital signal processing engine. The decimation filter process the oversampled data from the sigma-delta modulator to generate digital data at Nyquist sampling rate data with high dynamic range. The ADC supports sampling rates from 8KHz to 192KHz.



8.11 DAC

The DAC path includes a digital signal processing engine, a digital interpolation filter and a mono audio DAC, which uses a multi-bit digital delta-sigma modulator with a programmable oversampling ratio, an analog reconstruction filter and an output amplifier. The interpolation filter process the Nyquist sampling rate data to the sigma-delta modulator to generate oversampled rate data with high dynamic range. The DAC supports sampling rates from 8KHz to 192KHz.



8.12 Digital Signal Processing

The SS1311 offers an independent digital signal processing engine for the ADC and DAC. The signal processing engine includes a range of digital fixed-point processing blocks which implement various signal processing capabilities. All digital processing is done with 24-bit precision to minimize creation of processing artifacts and to maximize the audio dynamic range.

The ADC signal processing blocks available for user programming are:

• First-order HPF
• DVC Digital Volume control
• 1-band EQ
• 4-point DRC

The DAC signal processing blocks available for user programming are:

• DVC
• 3-band EQ
• 4-point DRC

8.12.1 HPF

A first-order high pass filter (HPF) is only used in the ADC path to remove DC bias levels or unnecessary low-frequency components from the ADC analog circuit. In microphone applications, the DC bias may cause significant pop noise, and the frequency signals below 100Hz cannot be fully reproduced, even cause "buzzing" noise, resulting in unnecessary low-frequency components.

The HPF is always recommended to be enabled. The -3dB cut-off frequency of this filter can be adjusted at the following frequencies by REG_0x1B: 1Hz, 10Hz, 20Hz, 70Hz and 200Hz.

8.12.2 DVC

The ADC and DAC have independent digital volume control (DVC). The DVC feature allows the volume to be adjusted from -95.5dB to +32dB in 0.5dB steps. A mute setting is included that will reduce the data to zero. In addition, users can choose the volume adjustment methods between zero-cross method and soft-volume method to prevent pop and click. The zero-cross method change the volume when the signal data is around 0. The soft-volume method ramps the volume up or down in the specific steps.

8.12.3 EQ

The SS1311 has 1-band parametric equalizer (EQ) in ADC path and 3-band EQ in DAC path. The EQ filter is a dedicated biquad filter with two poles and two zeros. Its transfer function is the Z-domain consists of two quadratic functions:

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

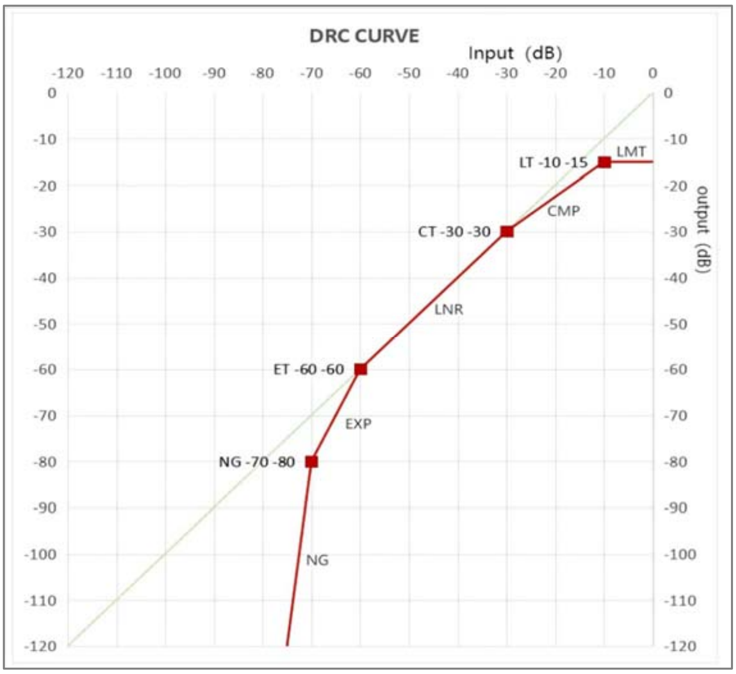
The coefficients a1 , a2, b0 , b1 , b2 are configurable for low-pass filter, high-pass filter, low-shelf filter, high-shelf filter, peak filter and notch filter, with various gain (aka "Q") and frequency controls.

Various types of filters have different uses. The biquad filter can configure high-pass filters intended for DC-blocking or low frequency noise reduction, such as reducing unwanted ambient noise or "wind noise" on a microphone input. Notch filters can also be configured to greatly reduce the noise at a specific frequency band or frequency, such as removing the power supply 60 Hz noise. Users can even achieve some simple sound effects with peak filter and shelf filter.

8.12.4 DRC

The ADC and DAC have independent 4-point dynamic range compressor (DRC). The DRC can be programmed to limit the maximum output level and/or boost a low output level. DRC static curve supports five sections: LMT, CMP, LNR, EXP, NG. Each sections is controlled by setting the slope and knee points in the registers.

- LMT Limiter section controlled by DRC_LMT_THD and DRC_LMT_SLP.
- CMP Compression section controlled by DRC_CMP_THD and DRC_CMP_SLP.
- LNR Linear section need no register control and the slope always be 1.
- EXP Expansion section controlled by DRC_EXP_THD and DRC_EXP_SLP.
- NG Noise-Gate section controlled by DRC_NG_THD and DRC_NG_SLP.



TIPS: LEADPOWER development team has provided an easy-to-use graphical tool to simplify software development on the EQ and DRC blocks. The graphical development environment can be dragged to achieve the desired effect with the click of a mouse.

8.13 Basic Setup Sequences

Example register setup to play 48K and record 16K

```
Ts{ iv$erh$gpsgo$gsrhmxmsr: $
① ZHHAZHHM$A727Z$
② Q GPOA:2588Q $FGPOAPVGO.:8A724;6Q $$PVGOA8<O$M6W$wpezi$q shi; $

Mrmxmep: $$$$$$$

3.hijeyp$stxmq m-exmsr.3$$
vikc{ vmxi,4|44$4|45-3$$33$Vikc4|44$A$4|45$viwix$xs$hijeyp$vikmwxiv$
vikc{ vmxi,4|5<$4|E4-3$$33$teh$hmwefpi$jsv$rsx$ywi$
vikc{ vmxi,4|<5$4|=6-3$$33$HEG$ieq t$eyxs$irefpi$
vikc{ vmxi,4|;I$4|::-3$$33$erepskcxyri5$
vikc{ vmxi,4|;J$4|96-3$$33$erepskcxyri6$
vikc{ vmxi,4|<9$4|4G-3$$33$erepskcxyri7$

Stir: $

3.$Ts{ iv$Sr$.3$
vikc{ vmxi,4|45$4|<h-3$$33$PHS$irefpi$
vikc{ vmxi,4|46$4|8=-3$$33$Q MGFMEW$irefpi$
3.$Gpsgo$hmz$.3$
vikc{ vmxi,4|4E$4|45-3$$33$W]WGPO$irefpi$
vikc{ vmxi,4|4G$4|69-3$$33$HEGcJWA8<O$EHGcJWA5:O$
vikc{ vmxi,4|4H$4|66-3$$33$EHGcGPO$
vikc{ vmxi,4|4I$4|64-3$$33$HEGcGPO$
vikc{ vmxi,4|4F$4|JJ-3$$33$GPO$kexmrk$hmwefpi$
3.$M6W$gsrjmk$.3$
vikc{ vmxi,4|54$4|47-3$$33$M6W$irefpi$
vikc{ vmxi,4|57$4|48-3$$33$M6W$jsvq ex$
3.$HEG$irefpi$.3$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
vikc{ vmxi,4|;E$4|E;-3$$33$EHG$erepsk$irefpi$$tkeckemrA74hF$
vikc{ vmxi,4|5E$4|4;-3$$33$EHG$hmkmxep$irefpi$
vikc{ vmxi,4|7E$4|47-3$$33$HEG$hmkmxep$irefpi$
vikc{ vmxi,4|<4$4|6F-3$$33$HEG$erepsk$irefpi$

Gpswi: $

3.$EHHE$hmwefpi$.3$
vikc{ vmxi,4|;E$4|E4-3$$33$EHG$erepsk$hmwefpi$
vikc{ vmxi,4|<4$4|6<-3$$33$HEG$erepsk$hmwefpi$
3.$vikmwxiv$viwix$.3$
vikc{ vmxi,4|44$4|45-3$$33$Vikc4|44$A$4|45$viwix$xs$hijeyp$vikmwxiv$
```

Register Maps

Register Name	Offset	Description
SRST	0x00	Soft Reset Register
PWR_CTRL1	0x01	Power Control Register 1
PWR_CTRL2	0x02	Power Control Register 2
PLL_CTRL	0x03	PLL Control Register 1
PLL_CFG1	0x04	PLL Configure Register 1
PLL_CFG2	0x05	PLL Configure Register 2
PLL_CFG3	0x06	PLL Configure Register 3
SYSCLK_CTRL	0x0A	System Clock Control Register
MODCLK_EN	0x0B	Module Clock Control Register
ADDA_FS	0x0C	ADDA Sampling Frequency Control Register
ADC_CLK_CTRL	0x0D	ADC Clock Control Register
DAC_CLK_CTRL	0x0E	DAC Clock Control Register
I2S_CTRL	0x10	I2S Control Register
I2S_FMT1	0x11	I2S Format Configure Register 1
I2S_FMT2	0x12	I2S Format Configure Register 2
I2S_FMT3	0x13	I2S Format Configure Register 3
I2S_TX_CTRL	0x14	I2S TX Control Register
I2S_RX_CTRL	0x15	I2S RX Control Register
I2S_TXM_CTRL	0x16	I2S TX Mixer Control Register
I2S_RXM_CTRL	0x17	I2S RX Mixer Control Register
I2S_PAD_CTRL	0x18	I2S PAD Control Register
ADC_DIG_CTRL	0x1A	ADC Digital Control Register
ADC_HPF_COEF	0x1B	ADC HPF Coefficient Register
ADC_DVC_CTRL	0x1C	ADC Digital Volume Control Register
ADC_SMUTE	0x1D	ADC Digital Soft-Mute Control Register
ADC_EQ_CTRL	0x20	ADC EQ Control Register
ADC_EQ1_b0	0x21-0x23	ADC EQ Band1 Coefficient b0
ADC_EQ1_b1	0x24-0x26	ADC EQ Band1 Coefficient b1
ADC_EQ1_b2	0x27-0x29	ADC EQ Band1 Coefficient b2
ADC_EQ1_a1	0x2A-0x2C	ADC EQ Band1 Coefficient a1
ADC_EQ1_a2	0x2D-0x2F	ADC EQ Band1 Coefficient a2
ADC_DRC_CTRL	0x30	ADC DRC Control Register
ADC_PEAK_CTRL	0x31	ADC DRC Peak Filter Control Register
ADC_ATK_TIME	0x32	ADC DRC ATK/DCY Time Register
ADC_DRC_THD1	0x33	ADC DRC Threshold Register 1
ADC_DRC_THD2	0x34	ADC DRC Threshold Register 2
ADC_DRC_THD3	0x35	ADC DRC Threshold Register 3
ADC_DRC_THD4	0x36	ADC DRC Threshold Register 4
ADC_DRC_SLP1	0x37	ADC DRC Slope Register 1
ADC_DRC_SLP2	0x38	ADC DRC Slope Register 2
DAC_DIG_CTRL	0x3A	DAC Digital Control Register
DAC_DVC_CTRL	0x3B	DAC Digital Volume Control Register
DAC_SMUTE	0x3C	DAC Digital Soft-Mute Control Register
DAC_DMIX_CTRL	0x3D	DAC Digital Mixer Control Register

DAC_EQ_CTRL	0x40	DAC EQ Control Register
DAC_EQ1_b0	0x41-0x43	DAC EQ Band1 Coefficient b0
DAC_EQ1_b1	0x44-0x46	DAC EQ Band1 Coefficient b1
DAC_EQ1_b2	0x47-0x49	DAC EQ Band1 Coefficient b2
DAC_EQ1_a1	0x4A-0x4C	DAC EQ Band1 Coefficient a1
DAC_EQ1_a2	0x4D-0x4F	DAC EQ Band1 Coefficient a2
DAC_EQ2_b0	0x51-0x53	DAC EQ Band2 Coefficient b0
DAC_EQ2_b1	0x54-0x56	DAC EQ Band2 Coefficient b1
DAC_EQ2_b2	0x57-0x59	DAC EQ Band2 Coefficient b2
DAC_EQ2_a1	0x5A-0x5C	DAC EQ Band2 Coefficient a1
DAC_EQ2_a2	0x5D-0x5F	DAC EQ Band2 Coefficient a2
DAC_EQ3_b0	0x61-0x63	DAC EQ Band3 Coefficient b0
DAC_EQ3_b1	0x64-0x66	DAC EQ Band3 Coefficient b1
DAC_EQ3_b2	0x67-0x69	DAC EQ Band3 Coefficient b2
DAC_EQ3_a1	0x6A-0x6C	DAC EQ Band3 Coefficient a1
DAC_EQ3_a2	0x6D-0x6F	DAC EQ Band3 Coefficient a2
DAC_DRC_CTRL	0x70	DAC DRC Control Register
DAC_PEAK_CTRL	0x71	DAC DRC Peak Filter Control Register
DAC_ATK_TIME	0x72	DAC DRC ATK/DCY Time Register
DAC_DRC_THD1	0x73	DAC DRC Threshold Register 1
DAC_DRC_THD2	0x74	DAC DRC Threshold Register 2
DAC_DRC_THD3	0x75	DAC DRC Threshold Register 3
DAC_DRC_THD4	0x76	DAC DRC Threshold Register 4
DAC_DRC_SLP1	0x77	DAC DRC Slope Register 1
DAC_DRC_SLP2	0x78	DAC DRC Slope Register 2
ANA_ADC_CTRL1	0x7A	ADC Analog Control Register 1
ANA_ADC_CTRL2	0x7B	ADC Analog Control Register 2
ANA_ADC_CTRL3	0x7C	ADC Analog Control Register 3
ANA_ADC_TUNE1	0x7E	ADC Analog Tuning Register 1
ANA_ADC_TUNE2	0x7F	ADC Analog Tuning Register 2
ANA_DAC_CTRL1	0x80	DAC Analog Control Register 1
ANA_DAC_CTRL2	0x81	DAC Analog Control Register 2
ANA_DAC_CTRL3	0x83	DAC Analog Control Register 3
ANA_DAC_TUNE1	0x84	DAC Analog Tuning Register 1
ANA_DAC_TUNE2	0x85	ADC Analog Tuning Register 2

Reg_0x00 Chip Soft Reset Register

Default: 0x00			Register Name: SRST
Bit	**Read/Write**	**Default**	**Description**
7:1	/	/	/
0	W1C	0x0	This bit controls system soft reset. When this bit sets to 1, all the register reset to the default value and the corresponding circuit reset to the default state except I2C. Returning the SRST bit to 0 is unnecessary; it is automatically set to 0 after triggering a system reset.

Reg_0x01 Power Control Register 1

Default: 0x8C			Register Name: PWR_CTRL1
Bit	**Read/Write**	**Default**	**Description**
7:5	R/W	0x4	Reserved
4	R/W	0x0	POWER_VREF_BYP VREF filter resistor bypass for test 0: not bypass 1: bypass
3:1	R/W	0x6	POWER_ALDO_VCTRL ALDO output voltage control 0: 1.6V 1: 1.65V 2:1.7V 3: 1.75V 4: 1.8V 5: 1.85V 6: 1.9V 7: 1.95V
0	R/W	0x0	POWER_ALDO_EN ALDO enable 0: Disable 1: Enable

Reg_0x02 Power Control Register 2

Default: 0x48			Register Name: PWR_CTRL2
Bit	**Read/Write**	**Default**	**Description**
7	R/W	0x0	POWER_MICBIAS_BYP MICBIAS regulator bypass 0: not bypass 1: bypass
6:4	R/W	0x4	POWER_ MICBIAS_CHOP_FREQ MICBIAS chop frequency control

			0: 24kHz 1: 48kHz 2: 96kHz 3: 192kHz 4: 384kHz 5: 768kHz 6: 1536kHz 7: 3072kHz
3	R/W	0x1	POWER_MICBIAS_CHOP_EN MICBIAS chop enable 0: Disable 1: Enable
2:1	R/W	0x0	POWER_MICBIAS_VCTRL MICBIAS output voltage control 0: 1.8V 1: 2.1V 2: 2.3V 3: 2.5V
0	R/W	0x0	POWER_MICBIAS_EN MICBIAS enable 0: Disable 1: Enable

Reg_0x03　PLL Control Register

Default: 0x48			**Register Name: PLL_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:4	R/W	0x4	Reserved
3:2	R/W	0x2	PLL_LDO_VCTRL PLL LDO output voltage control 0: 1.4V 1: 1.5V 2: 1.6V 3: 1.7V
1	R/W	0x0	PLL_LDO_EN PLL LDO circuit enable 0: Disable 1: Enable
0	R/W	0x0	PLL_EN PLL circuit enable 0: Disable 1: Enable

			The PLL output FOUT= FIN*N/(P*M)

Reg_0x04 PLL Configure Register 1

Default: 0x00			**Register Name: PLL_CFG1**
Bit	**Read/Write**	**Default**	**Description**
7:5	R/W	0x0	reserved
4:0	R/W	0x0	PLL_P_DIV PLL pre divider control P = PLL_P_DIV+1

Reg_0x05 PLL Configure Register 2

Default: 0x01			**Register Name: PLL_CFG2**
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x1	PLL_N_DIV PLL feedback divider control N = PLL_N_DIV+1 Note: PLL_N_DIV=0 excluded

Reg_0x06 PLL Configure Register 3

Default: 0x00			**Register Name: PLL_CFG3**
Bit	**Read/Write**	**Default**	**Description**
7:4	/	/	/
3:0	R/W	0x0	PLL_M_DIV PLL post divider control 0: M=2 1~15: M=2*PLL_M_DIV

Reg_0x0A System Clock Control Register

Default: 0x00			**Register Name: SYSCLK_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:5	R/W	0x0	Reserved
4	R/W	0x0	PLLCLK_SRC PLL Clock Source Select 0: MCLK 1: BCLK
3	R/W	0x0	PLLCLK_EN PLLCLK Enable 0: Disable 1: Enable

2:1	R/W	0x0	SYSCLK_SRC System Clock Source Select 0: MCLK 1: BCLK 2: PLL 3: Reserved
0	R/W	0x0	SYSCLK_EN SYSCLK Enable 0: Disable 1: Enable

Reg_0x0B Module Clock Control Register

Default: 0x00			Register Name: MODCLK_EN
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	MODCLK_EN Module Clock Enable 0: Disable 1: Enable BIT7: DAC_DSP_CLK (DAC Biquad/DRC clock) BIT6: DAC_DIGITAL_CLK (DAC digital clock) BIT5: DAC_ANALOG_CLK (DAC analog clock) BIT4: DAC_PATH_CLK (DAC path clock) BIT3: ADC_DSP_CLK (ADC Biquad/DRC clock) BIT2: ADC_DIGITAL_CLK (ADC digital clock) BIT1: ADC_ANALOG_CLK (ADC analog clock) BIT0: ADC_PATH_CLK (ADC path clock)

Reg_0x0C ADDA Sampling Frequency Control Register

Default: 0x25			Register Name: ADDA_FS
Bit	**Read/Write**	**Default**	**Description**
7	R/W	0x0	reserved
6:4	R/W	0x2	ADC_FS The ADC sample frequency 48K-series 44.1K-series 0: ADC_FS = 8K 1: ADC_FS = 12K 11.025K 2: ADC_FS = 16K 3: ADC_FS = 24K 22.05K 4: ADC_FS = 32K 5: ADC_FS = 48K 44.1K 6: ADC_FS = 96K 88.2K 7: ADC_FS = 192K 176.4K

3	R/W	0x0	reserved
2:0	R/W	0x5	DAC_FS The DAC sample frequency 48K-series 44.1K-series 0: DAC_FS = 8K 1: DAC_FS = 12K 11.025K 2: DAC_FS = 16K 3: DAC_FS = 24K 22.05K 4: DAC_FS = 32K 5: DAC_FS = 48K 44.1K 6: DAC_FS = 96K 88.2K 7: DAC_FS = 192K 176.4K

Reg_0x0D ADC Clock Control Register

Default: 0x20			**Register Name: ADC_CLK_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:6	/	/	/
5:4	R/W	0x2	ADC_OSR ADC oversampling Ratio 0: ADC_OSR= 32 1: ADC_OSR= 64 2: ADC_OSR= 128 3: ADC_OSR= 256
3:0	R/W	0x0	ADC_DIV The ADC oversampling CLK (ADC_DCLK) divide ratio from SYSCLK. The equation is ADC_DCLK = SYS_CLK / ADC_DIV. 0: ADC_DIV = 1 1: ADC_DIV = 2 2: ADC_DIV = 3 3: ADC_DIV = 4 4: ADC_DIV = 6 5: ADC_DIV = 8 6: ADC_DIV = 12 7: ADC_DIV = 16 8: ADC_DIV = 24 other: Reserved Note: The ADC_DCLK should be divided to be equal to ADC_OSR*ADC_FS.

Reg_0x0E DAC Clock Control Register

Default: 0x20	**Register Name: DAC_CLK_CTRL**

Bit	Read/Write	Default	Description
7:6	/	/	/
5:4	R/W	0x2	DAC_OSR DAC oversampling Ratio 0: DAC_OSR= 32 1: DAC_OSR= 64 2: DAC_OSR= 128 3: DAC_OSR= 256
3:0	R/W	0x0	DAC_DIV The DAC oversampling CLK (DAC_DCLK) divide ratio from SYS_CLK, The equation is DAC_DCLK = SYS_CLK / DAC_DIV. 0: DAC_DIV = 1 1: DAC_DIV = 2 2: DAC_DIV = 3 3: DAC_DIV = 4 4: DAC_DIV = 6 5: DAC_DIV = 8 6: DAC_DIV = 12 7: DAC_DIV = 16 8: DAC_DIV = 24 other: Reserved Note: The DAC_DCLK should be divided to be equal to DAC_OSR * DAC_FS.

Reg_0x10 I2S Control Register

Default: 0x00			**Register Name: I2S_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:6	R/W	0x0	MCLK_IO MCLK input or output select 0: Input 1: Output PDMCLK 2: Output SYSCLK 3: Input
5:4	R/W	0x0	reserved
3	R/W	0x0	I2S_MASTER I2S slave mode or master mode select 0: Slave Mode 1: Master Mode When I2S is in slave mode, BCLK and LRCK are used as inputs. When I2S is in master mode, BCLK and LRCK are used as outputs
2	R/W	0x0	I2S_TXEN

			I2S transmitter block enable 0: Disable 1: Enable
1	R/W	0x0	I2S_RXEN I2S receiver block enable 0: Disable 1: Enable
0	R/W	0x0	I2S_EN I2S interface enable 0: Disable 1: Enable

Reg_0x11 I2S Format Configure Register 1

Default: 0x00			**Register Name: I2S_FMT1**
Bit	**Read/Write**	**Default**	**Description**
7:4	/	/	/
3:0	R/W	0x0	BCLK_DIV BCLK Frequency divided from SYSCLK. The equation BCLK = SYSCLK/ BCLK_DIV. 0: BCLK_DIV = 1 1: BCLK_DIV = 2 2: BCLK_DIV = 3 3: BCLK_DIV = 4 4: BCLK_DIV = 6 5: BCLK_DIV = 8 6: BCLK_DIV = 12 7: BCLK_DIV = 16 8: BCLK_DIV = 24 9~15: reserved Note: This register is only used in master mode.

Reg_0x12 I2S Format Configure Register 2

Default: 0x3F			**Register Name: I2S_FMT2**
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x3F	LRCK_DIV LRCK Frequency divided from BCLK. The equation LRCK = BCLK/ (LRCK_DIV+1). For example: 0~30: Reserved 31: 32 BCLKs width 33: 34 BCLKs width

			35: 36 BCLKs width … 63: 64 BCLKs width … 255: 256 BCLKs width Note: The last bit of this register is always forced to 1. This register is only used in master mode.

Reg_0x13 I2S Format Configure Register 3

Default: 0x05			**Register Name: I2S_FMT3**
Bit	**Read/Write**	**Default**	**Description**
7	R/W	0x0	BCLK_POLARITY 0: not inverted 1: inverted
6	R/W	0x0	LRCK_POLARITY 0: not inverted 1: inverted
5:4	R/W	0x0	MODE_SEL Mode Selection 0: I2S_Standard mode (offset 1) 1: Left-Justified mode (offset 0) 2: PCM_A mode (offset 1) 3: PCM_B mode (offset 0)
3:2	R/W	0x1	WL Word Length 0: 16-bit 1: 20-bit 2: 24-bit 3: 32-bit
1	R/W	0x0	TX_WORD_HIZ 0: normal mode for the last half cycle of BCLK in the word 1: turn to hi-z state for the last half cycle of BCLK in the word
0	R/W	0x1	TX_STATE 0: transfer level 0 when not transferring word 1: turn to hi-z state when not transferring word

Reg_0x14 I2S TX Control Register

Default: 0x35			**Register Name: I2S_TX_CTRL**
Bit	**Read/Write**	**Default**	**Description**

7:6	/	/	/
5:4	R/W	0x3	TX_SLOTEN I2S interface TX data line slot enable. The bit[5:4] refer to slot[1:0]. When one or two slot is disabled, the affected slot of the I2S interface data line is set to hi-z state 0: Disable 1: Enable Note: only used for two chips drive the TX data line simultaneously
3	R/W	0x0	reserved
2	R/W	0x1	TX_SLOT1_MAP I2S interface TX data line slot 1 mapping source from TX left data or TX right data 0: TXL 1: TXR
1	R/W	0x0	TX_SLOT0_MAP I2S interface TX data line slot 0 mapping source from TX left data or TX right data 0: TXL 1: TXR
0	R/W	0x1	TX_SLOT_SEL I2S interface TX data line (SDOUT pin) slot number Select 0: 1 slot (channel) 1: 2 slot (channel) When TX_SLOT_SEL = 0, only slot 0 is active.

Reg_0x15 I2S RX Control Register

Default: 0x05			**Register Name: I2S_RX_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:3	/	/	/
2	R/W	0x1	RXR_MAP RX right data mapping source from I2S interface RX data line slot 0 or slot 1 0: slot0 1: slot1
1	R/W	0x0	RXL_MAP RX left data mapping source from I2S interface RX data line slot 0 or slot 1 0: slot0 1: slot1
0	R/W	0x1	RX_SLOT_SEL I2S interface RX data line (SDIN pin) slot number Select

			0: 1 slot (channel) 1: 2 slot (channel) When RX_SLOT_SEL = 0, only slot 0 is active. The slot 1 is not-used and received as 0 data.

Reg_0x16 I2S TX Mixer Control Register

Default: 0x11			**Register Name: I2S_TXM_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:6	R/W	0x0	TX_MIXR_GAIN I2S TX right mixer gain control 0: 0dB 1: -6dB Bit7: DAC_LOOP Bit6: ADC_DO
5:4	R/W	0x1	TX_MIXR_SRC I2S TX right mixer source control 0: Disable 1: Enable Bit5: DAC_LOOP Bit4: ADC_DO
3:2	R/W	0x0	TX_MIXL_GAIN I2S TX left mixer gain control 0: 0dB 1: -6dB Bit3: DAC_DI Bit2: ADC_DO
1:0	R/W	0x1	TX_MIXL_SRC I2S TX left mixer source control 0: Disable 1: Enable Bit1: DAC_DI Bit0: ADC_DO

Reg_0x17 I2S RX Mixer Control Register

Default: 0x01			**Register Name: I2S_RXM_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:4	/	/	/
3:2	R/W	0x0	RX_MIX_GAIN I2S RX mixer gain control 0: 0dB 1: -6dB Bit3: RXR Bit2: RXL
1:0	R/W	0x1	RX_MIX_SRC I2S RX mixer source control

			0: Disable 1: Enable Bit1: RXR Bit0: RXL

Reg_0x18 I2S PAD Control Register

Default: 0x80			**Register Name: I2S_PAD_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:6	R/W	0x2	I2S_PAD_DRL I2S pad drive level 0: Level 0 1: Level 1 2: Level 2 3: Level 3
5	R/W	0x0	DMICDAT_PAD_DIS DMICDAT pad disable 0: Enable 1: Disable
4	R/W	0x0	SDOUT_PAD_DIS SDOUT pad disable 0: Enable 1: Disable
3	R/W	0x0	SDIN_PAD_DIS SDIN pad disable 0: Enable 1: Disable
2	R/W	0x0	LRCK_PAD_DIS LRCK pad disable 0: Enable 1: Disable
1	R/W	0x0	BCLK_PAD_DIS BCLK pad disable 0: Enable 1: Disable
0	R/W	0x0	MCLK_PAD_DIS MCLK pad disable 0: Enable 1: Disable

Reg_0x1A ADC Digital Control Register

Default: 0x06	**Register Name: ADC_DIG_CTRL**

Bit	Read/Write	Default	Description
7	R/W	0x0	PDM_IO PDM IO multiplexing function select 0: input as DEVICE_ID 1: output as PDMCLK
6:5	R/W	0x0	ADOUT_DLY ADC Delay Function enable for transmitting data after ADC_DIG_EN 00: 0ms 01: 4ms 10: 8ms 11: 16ms
4	R/W	0x0	PDM_TIMING PDM timing control 0: Latch left channel data on rising clock edge. Latch right channel data on falling clock edge. 1: Latch left channel data on falling clock edge. Latch right channel data on rising clock edge.
3	R/W	0x0	PDM_EN PDM interface Enable 0: Disable 1: Enable
2	R/W	0x1	ADC_HPF_EN ADC digital HPF enable 0: DisableS 1: Enable
1	R/W	0x1	ADC_DITHEN ADC dithering enable 0: Disable 1: Enable
0	R/W	0x0	ADC_DIG_EN ADC digital part enable 0: Disable 1: Enable

Reg_0x1B ADC HPF Coefficient Register

Default: 0x00			**Register Name: ADC_HPF_COEF**
Bit	**Read/Write**	**Default**	**Description**
7:3	/	/	/
2:0	R/W	0x0	ADC_COEF 0：1Hz 1：10Hz

			2：20Hz 3：70Hz 4：200Hz others：Reserved

Reg_0x1C ADC Digital Volume Control Register

Default: 0xBF			**Register Name: ADC_DVC_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0xBF	ADC_DIG_VOL ADC Digital Volume Control (-95dB to 32dB, 0.5dB/Step) 0x00: Mute 0x01: -95dB … 0.5dB/step 0xBE: -0.5dB 0xBF: 0dB (default) 0xC0: +0.5dB … 0xFF: +32dB

Reg_0x1D ADC Digital Soft-Mute Control Register

Default: 0x10			**Register Name: ADC_SMUTE**
Bit	**Read/Write**	**Default**	**Description**
7:5	/	/	/
4	R/W	0x1	ADC_ZERO_CROSS ADC zero-cross enable 0 = Disable 1 = Enable
3:1	R/W	0x0	ADC_SOFT_VOL_RATE ADC volume ramp rate with n ADC sample frequency cycle per step 0: 4 sample frequency 1: 8 sample frequency 2: 16 sample frequency 3: 32 sample frequency 4: 64 sample frequency 5: 128 sample frequency 6: 256 sample frequency 7: 512 sample frequency
0	R/W	0x0	ADC_SOFT_VOL_EN ADC soft volume enable 0 = Disable

			1 = Enable This bit has a higher priority than ZERO_CROSS bit

Reg_0x20 ADC EQ Control Register

Default: 0x00			Register Name: ADC_EQ_CTRL
Bit	**Read/Write**	**Default**	**Description**
7:1	/	/	/
0	R/W	0x0	ADC_EQ1_EN ADC band-1 EQ enable 0: Disable 1: Enable

Reg_0x21 ADC EQ Band1 Coefficient b0 Register 1

Default: 0x00			Register Name: ADC_EQ1_b0[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_b0[23:16] ADC EQ band-1 coefficient b0 setting

Reg_0x22 ADC EQ Band1 Coefficient b0 Register 2

Default: 0x00			Register Name: ADC_EQ1_b0[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_b0[15:8] ADC EQ band-1 coefficient b0 setting

Reg_0x23 ADC EQ Band1 Coefficient b0 Register 3

Default: 0x00			Register Name: ADC_EQ1_b0[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_b0[7:0] ADC EQ band-1 coefficient b0 setting

Reg_0x24 ADC EQ Band1 Coefficient b1 Register 1

Default: 0x00			Register Name: ADC_EQ1_b1[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_b1[23:16] ADC EQ band-1 coefficient b1 setting

Reg_0x25 ADC EQ Band1 Coefficient b1 Register 2

Default: 0x00			Register Name: ADC_EQ1_b1[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_b1[15:8] ADC EQ band-1 coefficient b1 setting

Reg_0x26 ADC EQ Band1 Coefficient b1 Register 3

Default: 0x00			Register Name: ADC_EQ1_b1[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_b1[7:0] ADC EQ band-1 coefficient b1 setting

Reg_0x27 ADC EQ Band1 Coefficient b2 Register 1

Default: 0x00			Register Name: ADC_EQ1_b2[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_b2[23:16] ADC EQ band-1 coefficient b2 setting

Reg_0x28 ADC EQ Band1 Coefficient b2 Register 2

Default: 0x00			Register Name: ADC_EQ1_b2[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_b2[15:8] ADC EQ band-1 coefficient b2 setting

Reg_0x29 ADC EQ Band1 Coefficient b2 Register 3

Default: 0x00			Register Name: ADC_EQ1_b2[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_b2[7:0] ADC EQ band-1 coefficient b2 setting

Reg_0x2A ADC EQ Band1 Coefficient a1 Register 1

Default: 0x00			Register Name: ADC_EQ1_a1[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_a1[23:16] ADC EQ band-1 coefficient a1 setting

Reg_0x2B ADC EQ Band1 Coefficient a1 Register 2

Default: 0x00			Register Name: ADC_EQ1_a1[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_a1[15:8] ADC EQ band-1 coefficient a1 setting

Reg_0x2C ADC EQ Band1 Coefficient a1 Register 3

Default: 0x00			Register Name: ADC_EQ1_a1[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_a1[7:0] ADC EQ band-1 coefficient a1 setting

Reg_0x2D ADC EQ Band1 Coefficient a2 Register 1

Default: 0x00			Register Name: ADC_EQ1_a2[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_a2[23:16] ADC EQ band-1 coefficient a2 setting

Reg_0x2E ADC EQ Band1 Coefficient a2 Register 2

Default: 0x00			Register Name: ADC_EQ1_a2[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_a2[15:8] ADC EQ band-1 coefficient a2 setting

Reg_0x2F ADC EQ Band1 Coefficient a2 Register 3

Default: 0x00			Register Name: ADC_EQ1_a2[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	ADC_EQ1_a2[7:0] ADC EQ band-1 coefficient a2 setting

Reg_0x30 ADC DRC Control Register

Default: 0x02			Register Name: ADC_DRC_CTRL
Bit	**Read/Write**	**Default**	**Description**
7:3	/	/	/
2	R/W	0x0	ADC_DRC_SMTH_MODE ADC DRC smooth filter mode 0: Improved attacking and releasing process

			1: Traditional process
1	R/W	0x1	ADC_DRC_SMTH_EN ADC DRC smooth filter enable, when disabled, data should be bypassed directly 0: Disable 1: Enable
0	R/W	0x0	ADC_DRC_EN ADC DRC enable, when DRC is disabled, data should be bypassed directly to output 0: Disable 1: Enable

Reg_0x31 ADC DRC Peak Filter Control Register

Default: 0x16			**Register Name: ADC_PEAK_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:4	R/W	0x01	ADC_DRC_PEAK_AT ADC DRC peak filter attack time control 4'd0: Ts*1 4'd1: Ts*2 4'd2: Ts*4 4'd3: Ts*8 4'd4: Ts*16 4'd5: Ts*32 4'd6: Ts*64 4'd7: Ts*128 4'd8: Ts*256 4'd9: Ts*1024 others: Ts*1024
3:0	R/W	0x06	ADC_DRC_PEAK_RT ADC DRC peak filter release time control 4'd0: Ts*64 4'd1: Ts*128 4'd2: Ts*256 4'd3: Ts*512 4'd4: Ts*1024 4'd5: Ts*2048 4'd6: Ts*4096 4'd7: Ts*8192 4'd8: Ts*16384 4'd9: Ts*32768 others: Ts*32768

Reg_0x32 ADC DRC ATK/DCY Time Register

Default: 0x27			**Register Name: ADC_ATK_TIME**
Bit	**Read/Write**	**Default**	**Description**
7:4	R/W	0x02	ADC_ATK_TIME ADC DRC attack time control 4'd0: Ts*2 4'd1: Ts*4 4'd2: Ts*8 4'd3: Ts*16 4'd4: Ts*32 4'd5: Ts*64 4'd6: Ts*128 4'd7: Ts*256 4'd8: Ts*512 4'd9: Ts*1024 4'd10: Ts*2048 4'd11: Ts*4096 others: Ts*4096
3:0	R/W	0x07	ADC_DCY_TIME ADC DRC decay time control 4'd0: Ts*64 4'd1: Ts*128 4'd2: Ts*256 4'd3: Ts*512 4'd4: Ts*1024 4'd5: Ts*2048 4'd6: Ts*4096 4'd7: Ts*8192 4'd8: Ts*16384 4'd9: Ts*32768 4'd10: Ts*65536 4'd11: Ts*131072 others: Ts*131072

Reg_0x33 ADC DRC Threshold Register 1

Default: 0x02			**Register Name: ADC_DRC_THD1**
Bit	**Read/Write**	**Default**	**Description**
7:5	/	/	/
4:0	R/W	0x02	ADC_DRC_LMT_THD ADC DRC limiter threshold, step size 1dB, range [-31dB,0dB]

			5'd0: 0dB 5'd1: -1dB … 5'd30: -30dB 5'd31: -31dB threshold = -unsigned(reg)

Reg_0x34 ADC DRC Threshold Register 2

Default: 0x0A			Register Name: ADC_DRC_THD2
Bit	**Read/Write**	**Default**	**Description**
7:6	/	/	/
5:0	R/W	0x0A	ADC_DRC_CMP_THD ADC DRC compressor threshold, step size 1dB, range [-63dB,0dB] 6'd0: 0dB 6'd1: -1dB … 6'd62: -62dB 6'd63: -63dB threshold = -unsigned(reg)

Reg_0x35 ADC DRC Threshold Register 3

Default: 0x16			Register Name: ADC_DRC_THD3
Bit	**Read/Write**	**Default**	**Description**
7:6	/	/	/
5:0	R/W	0x16	ADC_DRC_EXP_THD ADC DRC expander threshold, step size 1dB, range [-81dB,-18dB] 6'd0: -18dB 6'd1: -19dB … 6'd62: -80dB 6'd63: -81dB threshold = -unsigned(reg)-18dB

Reg_0x36 ADC DRC Threshold Register 4

Default: 0x0F			Register Name: ADC_DRC_THD4
Bit	**Read/Write**	**Default**	**Description**
7:6	/	/	/
5:0	R/W	0x0F	ADC_DRC_NG_THD ADC DRC noise gate threshold, step size 1dB, range [-98dB,-35dB] 6'd0: -35dB

			6'd1: -36dB … 6'd62: -97dB 6'd63: -98dB threshold = -unsigned(reg)-35dB

Reg_0x37 ADC DRC Slope Register 1

Default: 0x72			**Register Name: ADC_DRC_SLP1**
Bit	**Read/Write**	**Default**	**Description**
7	/	/	/
6:4	R/W	0x07	ADC_DRC_LMT_SLP ADC DRC limiter slope 0: 1/1 1: 1/2 2: 1/4 3: 1/8 4: 1/16 5: 1/32 6: 1/64 7: 0/1
3	/	/	Reserved
2:0	R/W	0x02	ADC_DRC_CMP_SLP ADC DRC compressor slope 0: 1/1 1: 3/4 2: 1/2 3: 1/4 4: 1/8 5: 1/16 6: 1/32 7: 0/1

Reg_0x38 ADC DRC Slope Register 2

Default: 0x70			**Register Name: ADC_DRC_SLP2**
Bit	**Read/Write**	**Default**	**Description**
7:6	R/W	0x01	ADC_DRC_EXP_SLP ADC DRC expander slope 0: 1/1 1: 2/1 2: 4/1 3: 8/1

5:4	R/W	0x03	ADC_DRC_NG_SLP ADC DRC noise gate slope 0: 1/1 1: 2/1 2: 4/1 3: 8/1
3:0	R/W	0x00	ADC_DRC_GAIN ADC DRC makeup gain, step size 1dB, range [0dB,15dB] 4'd0: 0dB 4'd1: 1dB … 4'd14: 14dB 4'd15: 15dB gainboost = unsigned(reg)

Reg_0x3A DAC Digital Control Register

Default: 0x06			Register Name: DAC_DIG_CTRL
Bit	**Read/Write**	**Default**	**Description**
7:4	/	/	/
3:2	R/W	0x1	DAC_DITHSEL DAC dithering amplitude selection 0: dither amp=1/8LSB 1: dither amp=2/8LSB 2: dither amp=3/8LSB 3: dither amp=4/8LSB
1	R/W	0x1	DAC_DITHEN DAC dithering enable 0: Disable 1: Enable
0	R/W	0x0	DAC_DIG_EN DAC Digital part enable 0: Disable 1: Enable

Reg_0x3B DAC Digital Volume Control Register

Default: 0xBF			Register Name: DAC_DVC_CTRL
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0xBF	DAC_ DIG_VOL DAC Digital Volume Control (-95dB to 32dB, 0.5dB/Step) 0x00: Mute

			0x01: -95dB … 0.5dB/step 0xBE: -0.5dB 0xBF: 0dB (default) 0xC0: +0.5dB … 0xFF: +32dB

Reg_0x3C DAC Digital Soft-Mute Control Register

Default: 0x10			**Register Name: DAC_SMUTE**
Bit	**Read/Write**	**Default**	**Description**
7:6	/	/	/
5	R/W	0x0	DAC_AMUTE_EN DAC auto mute enable 0 = Disable 1 = Enable
4	R/W	0x1	DAC_ZERO_CROSS DAC zero-cross enable 0 = Disable 1 = Enable
3:1	R/W	0x0	DAC_SOFT_VOL_RATE DAC volume ramp rate with n DAC sample frequency cycle per step 0: 4 sample frequency 1: 8 sample frequency 2: 16 sample frequency 3: 32 sample frequency 4: 64 sample frequency 5: 128 sample frequency 6: 256 sample frequency 7: 512 sample frequency
0	R/W	0x0	DAC_SOFT_VOL_EN DAC Soft volume enable 0 = Disable 1 = Enable This bit has a higher priority than ZERO_CROSS bit

Reg_0x3D DAC Digital Mixer Control Register

Default: 0x01			**Register Name: DAC_DMIX_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:4	/	/	/

3:2	R/W	0x0	DAC_DMX_GAIN DAC digital mixer gain control 0: 0dB 1: -6dB Bit3: ADC_DO data Bit2: DAC_DI data
1:0	R/W	0x1	DAC_DMX_SRC DAC digital mixer source select 0: Disable 1: Enable Bit1: ADC_DO data Bit0: DAC_DI data

Reg_0x40 DAC EQ Control Register

Default: 0x00			**Register Name: DAC_EQ_CTRL**
Bit	**Read/Write**	**Default**	**Description**
7:3	/	/	/
2	R/W	0x0	DAC_EQ3_EN DAC band-3 EQ enable 0: Disable 1: Enable
1	R/W	0x0	DAC_EQ2_EN DAC band-2 EQ enable 0: Disable 1: Enable
0	R/W	0x0	DAC_EQ1_EN DAC band-1 EQ enable 0: Disable 1: Enable

Reg_0x41 DAC EQ Band1 Coefficient b0 Register 1

Default: 0x00			**Register Name: DAC_EQ1_b0[23:16]**
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_b0[23:16] DAC EQ band-1 coefficient b0 setting

Reg_0x42 DAC EQ Band1 Coefficient b0 Register 2

Default: 0x00			**Register Name: DAC_EQ1_b0[15:8]**
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_b0[15:8]

			DAC EQ band-1 coefficient b0 setting

Reg_0x43 DAC EQ Band1 Coefficient b0 Register 3

Default: 0x00			Register Name: DAC_EQ1_b0[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_b0[7:0] DAC EQ band-1 coefficient b0 setting

Reg_0x44 DAC EQ Band1 Coefficient b1 Register 1

Default: 0x00			Register Name: DAC_EQ1_b1[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_b1[23:16] DAC EQ band-1 coefficient b1 setting

Reg_0x45 DAC EQ Band1 Coefficient b1 Register 2

Default: 0x00			Register Name: DAC_EQ1_b1[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_b1[15:8] DAC EQ band-1 coefficient b1 setting

Reg_0x46 DAC EQ Band1 Coefficient b1 Register 3

Default: 0x00			Register Name: DAC_EQ1_b1[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_b1[7:0] DAC EQ band-1 coefficient b1 setting

Reg_0x47 DAC EQ Band1 Coefficient b2 Register 1

Default: 0x00			Register Name: DAC_EQ1_b2[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_b2[23:16] DAC EQ band-1 coefficient b2 setting

Reg_0x48 DAC EQ Band1 Coefficient b2 Register 2

Default: 0x00			Register Name: DAC_EQ1_b2[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_b2[15:8] DAC EQ band-1 coefficient b2 setting

Reg_0x49 DAC EQ Band1 Coefficient b2 Register 3

Default: 0x00			Register Name: DAC_EQ1_b2[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_b2[7:0] DAC EQ band-1 coefficient b2 setting

Reg_0x4A DAC EQ Band1 Coefficient a1 Register 1

Default: 0x00			Register Name: DAC_EQ1_a1[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_a1[23:16] DAC EQ band-1 coefficient a1 setting

Reg_0x4B DAC EQ Band1 Coefficient a1 Register 2

Default: 0x00			Register Name: DAC_EQ1_a1[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_a1[15:8] DAC EQ band-1 coefficient a1 setting

Reg_0x4C DAC EQ Band1 Coefficient a1 Register 3

Default: 0x00			Register Name: DAC_EQ1_a1[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_a1[7:0] DAC EQ band-1 coefficient a1 setting

Reg_0x4D DAC EQ Band1 Coefficient a2 Register 1

Default: 0x00			Register Name: DAC_EQ1_a2[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_a2[23:16] DAC EQ band-1 coefficient a2 setting

Reg_0x4E DAC EQ Band1 Coefficient a2 Register 2

Default: 0x00			Register Name: DAC_EQ1_a2[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_a2[15:8] DAC EQ band-1 coefficient a2 setting

Reg_0x4F DAC EQ Band1 Coefficient a2 Register 3

Default: 0x00			Register Name: DAC_EQ1_a2[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_a2[7:0] DAC EQ band-1 coefficient a2 setting

Reg_0x51 DAC EQ Band2 Coefficient b0 Register 1

Default: 0x00			Register Name: DAC_EQ2_b0[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_b0[23:16] DAC EQ band-2 coefficient b0 setting

Reg_0x52 DAC EQ Band2 Coefficient b0 Register 2

Default: 0x00			Register Name: DAC_EQ2_b0[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_b0[15:8] DAC EQ band-2 coefficient b0 setting

Reg_0x53 DAC EQ Band2 Coefficient b0 Register 3

Default: 0x00			Register Name: DAC_EQ2_b0[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_b0[7:0] DAC EQ band-2 coefficient b0 setting

Reg_0x54 DAC EQ Band2 Coefficient b1 Register 1

Default: 0x00			Register Name: DAC_EQ2_b1[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ1_b2[23:16] DAC EQ band-2 coefficient b1 setting

Reg_0x55 DAC EQ Band2 Coefficient b1 Register 2

Default: 0x00			Register Name: DAC_EQ2_b1[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_b1[15:8] DAC EQ band-2 coefficient b1 setting

Reg_0x56 DAC EQ Band2 Coefficient b1 Register 3

Default: 0x00			Register Name: DAC_EQ2_b1[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_b1[7:0] DAC EQ band-2 coefficient b1 setting

Reg_0x57 DAC EQ Band2 Coefficient b2 Register 1

Default: 0x00			Register Name: DAC_EQ2_b2[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_b2[23:16] DAC EQ band-2 coefficient b2 setting

Reg_0x58 DAC EQ Band2 Coefficient b2 Register 2

Default: 0x00			Register Name: DAC_EQ2_b2[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_b2[15:8] DAC EQ band-2 coefficient b2 setting

Reg_0x59 DAC EQ Band2 Coefficient b2 Register 3

Default: 0x00			Register Name: DAC_EQ2_b2[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_b2[7:0] DAC EQ band-2 coefficient b2 setting

Reg_0x5A DAC EQ Band2 Coefficient a1 Register 1

Default: 0x00			Register Name: DAC_EQ2_a1[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_a1[23:16] DAC EQ band-2 coefficient a1 setting

Reg_0x5B DAC EQ Band2 Coefficient a1 Register 2

Default: 0x00			Register Name: DAC_EQ2_a1[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_a1[15:8] DAC EQ band-2 coefficient a1 setting

Reg_0x5C DAC EQ Band2 Coefficient a1 Register 3

Default: 0x00			Register Name: DAC_EQ2_a1[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_a1[7:0] DAC EQ band-2 coefficient a1 setting

Reg_0x5D DAC EQ Band2 Coefficient a2 Register 1

Default: 0x00			Register Name: DAC_EQ2_a2[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_a2[23:16] DAC EQ band-2 coefficient a2 setting

Reg_0x5E DAC EQ Band2 Coefficient a2 Register 2

Default: 0x00			Register Name: DAC_EQ2_a2[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_a2[15:8] DAC EQ band-2 coefficient a2 setting

Reg_0x5F DAC EQ Band2 Coefficient a2 Register 3

Default: 0x00			Register Name: DAC_EQ2_a2[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ2_a2[7:0] DAC EQ band-2 coefficient a2 setting

Reg_0x61 DAC EQ Band3 Coefficient b0 Register 1

Default: 0x00			Register Name: DAC_EQ3_b0[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_b0[23:16] DAC EQ band-3 coefficient b0 setting

Reg_0x62 DAC EQ Band3 Coefficient b0 Register 2

Default: 0x00			Register Name: DAC_EQ3_b0[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_b0[15:8] DAC EQ band-3 coefficient b0 setting

Reg_0x63 DAC EQ Band3 Coefficient b0 Register 3

Default: 0x00			Register Name: DAC_EQ3_b0[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_b0[7:0] DAC EQ band-3 coefficient b0 setting

Reg_0x64 DAC EQ Band3 Coefficient b1 Register 1

Default: 0x00			Register Name: DAC_EQ3_b1[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_b1[23:16] DAC EQ band-3 coefficient b1 setting

Reg_0x65 DAC EQ Band3 Coefficient b1 Register 2

Default: 0x00			Register Name: DAC_EQ3_b1[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_b1[15:8] DAC EQ band-3 coefficient b1 setting

Reg_0x66 DAC EQ Band3 Coefficient b1 Register 3

Default: 0x00			Register Name: DAC_EQ3_b1[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_b1[7:0] DAC EQ band-3 coefficient b1 setting

Reg_0x67 DAC EQ Band3 Coefficient b2 Register 1

Default: 0x00			Register Name: DAC_EQ3_b2[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_b2[23:16] DAC EQ band-3 coefficient b2 setting

Reg_0x68 DAC EQ Band3 Coefficient b2 Register 2

Default: 0x00			Register Name: DAC_EQ3_b2[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_b2[15:8] DAC EQ band-3 coefficient b2 setting

Reg_0x69 DAC EQ Band3 Coefficient b2 Register 3

Default: 0x00			Register Name: DAC_EQ3_b2[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_b2[7:0] DAC EQ band-3 coefficient b2 setting

Reg_0x6A DAC EQ Band3 Coefficient a1 Register 1

Default: 0x00			Register Name: DAC_EQ3_a1[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_a1[23:16] DAC EQ band-3 coefficient a1 setting

Reg_0x6B DAC EQ Band3 Coefficient a1 Register 2

Default: 0x00			Register Name: DAC_EQ3_a1[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_a1[15:8] DAC EQ band-3 coefficient a1 setting

Reg_0x6C DAC EQ Band3 Coefficient a1 Register 3

Default: 0x00			Register Name: DAC_EQ3_a1[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_a1[7:0] DAC EQ band-3 coefficient a1 setting

Reg_0x6D DAC EQ Band3 Coefficient a2 Register 1

Default: 0x00			Register Name: DAC_EQ3_a2[23:16]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_a2[23:16] DAC EQ band-3 coefficient a2 setting

Reg_0x6E DAC EQ Band3 Coefficient a2 Register 2

Default: 0x00			Register Name: DAC_EQ3_a2[15:8]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_a2[15:8] DAC EQ band-3 coefficient a2 setting

Reg_0x6F DAC EQ Band3 Coefficient a2 Register 3

Default: 0x00			Register Name: DAC_EQ3_a2[7:0]
Bit	**Read/Write**	**Default**	**Description**
7:0	R/W	0x0	DAC_EQ3_a2[7:0] DAC EQ band-3 coefficient a2 setting

Reg_0x70 DAC DRC Control Register

Default: 0x02			Register Name: DAC_DRC_CTL
Bit	**Read/Write**	**Default**	**Description**
7:3	/	/	/
2	R/W	0x0	DAC_DRC_SMTH_MODE DAC DRC smooth filter mode 0: improved attacking and releasing process 1: traditional process
1	R/W	0x1	DAC_DRC_SMTH_EN DAC DRC smooth filter enable, when disabled, data should be bypassed directly 0: Disable 1: Enable
0	R/W	0x0	DAC_DRC_EN DAC DRC enable, when DRC is disabled, data should be bypassed directly to output 0: Disable 1: Enable

Reg_0x71 DAC DRC Peak Filter Control Register

Default: 0x16			Register Name: DAC_PEAK_CTL
Bit	**Read/Write**	**Default**	**Description**
7:4	R/W	0x01	DAC_DRC_PEAK_AT DAC DRC peak filter attack time control 4'd0: Ts*1 4'd1: Ts*2 4'd2: Ts*4 4'd3: Ts*8 4'd4: Ts*16 4'd5: Ts*32 4'd6: Ts*64 4'd7: Ts*128

			4'd8: Ts*256 4'd9: Ts*1024 others: Ts*1024
3:0	R/W	0x06	DAC_DRC_PEAK_RT DAC DRC peak filter release time control 4'd0: Ts*64 4'd1: Ts*128 4'd2: Ts*256 4'd3: Ts*512 4'd4: Ts*1024 4'd5: Ts*2048 4'd6: Ts*4096 4'd7: Ts*8192 4'd8: Ts*16384 4'd9: Ts*32768 others: Ts*32768

Reg_0x72 DAC DRC ATK/DCY Time Register

Default: 0x27			**Register Name: DAC_ATK_TIME**
Bit	**Read/Write**	**Default**	**Description**
7:4	R/W	0x02	DAC_ATK_TIME DAC DRC attack time control 4'd0: Ts*2 4'd1: Ts*4 4'd2: Ts*8 4'd3: Ts*16 4'd4: Ts*32 4'd5: Ts*64 4'd6: Ts*128 4'd7: Ts*256 4'd8: Ts*512 4'd9: Ts*1024 4'd10: Ts*2048 4'd11: Ts*4096 others: Ts*4096
3:0	R/W	0x07	DAC_DCY_TIME DAC DRC decay time control 4'd0: Ts*64 4'd1: Ts*128 4'd2: Ts*256 4'd3: Ts*512 4'd4: Ts*1024

			4'd5: Ts*2048 4'd6: Ts*4096 4'd7: Ts*8192 4'd8: Ts*16384 4'd9: Ts*32768 4'd10: Ts*65536 4'd11: Ts*131072 others: Ts*131072

Reg_0x73　DAC DRC Threshold Register 1

Default: 0x02			**Register Name: DAC_DRC_THD1**
Bit	**Read/Write**	**Default**	**Description**
7:5	/	/	/
4:0	R/W	0x02	DAC_DRC_LMT_THD DAC DRC limiter threshold, step size 1dB, range [-31dB,0dB] 5‘d0: 0dB 5'd1: -1dB … 5'd30: -30dB 5'd31: -31dB threshold = -unsigned(reg)

Reg_0x74　DAC DRC Threshold Register 2

Default: 0x0A			**Register Name: DAC_DRC_THD2**
Bit	**Read/Write**	**Default**	**Description**
7:6	/	/	/
5:0	R/W	0x0A	DAC_DRC_CMP_THD DAC DRC compressor threshold, step size 1dB, range [-63dB,0dB] 6‘d0: 0dB 6'd1: -1dB … 6'd62: -62dB 6'd63: -63dB threshold = -unsigned(reg)

Reg_0x75　DAC DRC Threshold Register 3

Default: 0x16			Register Name: DAC_DRC_THD3
Bit	**Read/Write**	**Default**	**Description**
7:6	/	/	/
5:0	R/W	0x16	DAC_DRC_EXP_THD DAC DRC expander threshold, step size 1dB, range [-81dB,-18dB] 6‘d0: -18dB 6'd1: -19dB … 6'd62: -80dB 6'd63: -81dB threshold = -unsigned(reg)-18dB

Reg_0x76　DAC DRC Threshold Register 4

Default: 0x0F			Register Name: DAC_DRC_THD4
Bit	**Read/Write**	**Default**	**Description**
7:6	/	/	/
5:0	R/W	0x0F	DAC_DRC_NG_THD DAC DRC noise gate threshold, step size 1dB, range [-98dB,-35dB] 6‘d0: -35dB 6'd1: -36dB … 6'd62: -97dB 6'd63: -98dB threshold = -unsigned(reg)-35dB

Reg_0x77　DAC DRC Slope Register 1

Default: 0x72			Register Name: DAC_DRC_SLP1
Bit	**Read/Write**	**Default**	**Description**
7	/	/	/
6:4	R/W	0x07	DAC_DRC_LMT_SLP DAC DRC limiter slope 0: 1/1 1: 1/2 2: 1/4 3: 1/8 4: 1/16 5: 1/32 6: 1/64 7: 0/1
3	/	/	Reserved

2:0	R/W	0x02	DAC_DRC_CMP_SLP DAC DRC compressor slope 0: 1/1 1: 3/4 2: 1/2 3: 1/4 4: 1/8 5: 1/16 6: 1/32 7: 0/1

Reg_0x78　DAC DRC Slope Register 2

Default: 0x70			**Register Name: DAC_DRC_SLP2**
Bit	**Read/Write**	**Default**	**Description**
7:6	R/W	0x01	DAC_DRC_EXP_SLP DAC DRC expander slope 0: 1/1 1: 2/1 2: 4/1 3: 8/1
5:4	R/W	0x03	DAC_DRC_NG_SLP DAC DRC noise gate slope 0: 1/1 1: 2/1 2: 4/1 3: 8/1
3:0	R/W	0x00	DAC_DRC_GAIN DAC DRC makeup gain, step size 1dB, range [0dB,15dB] 4'd0: 0dB 4'd1: 1dB … 4'd14: 14dB 4'd15: 15dB gainboost = unsigned(reg)

Reg_0x7A　ADC Analog Control Register 1

Default:0x00			**Register Name: ANA_ADC_CTRL1**
Bit	**R/W**	**Default**	**Description**
7:4	R/W	0x0	ADC_GAIN ADC PGA Gain control, 3dB/step 4'd0: 0dB

			4'd1: 0dB 4'd2: 6dB 4'd3: 9dB … 4'd14: 42dB 4'd15: 42dB
3	R/W	0x0	Reserved
2	R/W	0x0	ADC_CONV_EN ADC SDM conversion start signal enable 0: Disable 1: Enable
1	R/W	0x0	ADC_SDM_EN ADC SDM related circuit enable 0: Disable 1: Enable
0	R/W	0x0	ADC_PGA_EN ADC PGA enable 0: Disable 1: Enable

Reg_0x7B ADC Analog Control Register 2

Default:0x29			**Register Name: ANA_ADC_CTRL2**
Bit	**R/W**	**Default**	**Description**
7	R/W	0x0	Reserved
6	R/W	0x0	ADC_PGA_FAST_SET ADC PGA high-pass filter fast settling control, when set to 1, high-pass will be settled in 15ms@1uF or 2ms@100nF 0: Disable 1: Enable
5:0	R/W	0x29	ADC_PGA_OPTIMIZE ADC PGA optimize control

Reg_0x7C ADC Analog Control Register 3

Default:0xFF			**Register Name: ANA_ADC_CTRL3**
Bit	**R/W**	**Default**	**Description**
7:4	R/W	0xF	Reserved
3:0	R/W	0xF	ADC_SDM_OPTIMIZE ADC SDM optimize control

Reg_0x7E ADC Analog Tuning Register 1

Default:0x7E			Register Name: ANA_ADC_TUNE1
Bit	**R/W**	**Default**	**Description**
7:0	R/W	0x7E	ADC analog tuning

Reg_0x7F ADC Analog Tuning Register 2

Default:0x5A			Register Name: ANA_ADC_TUNE2
Bit	**R/W**	**Default**	**Description**
7:0	R/W	0x5A	ADC analog tuning

Reg_0x80 DAC Analog Control Register 1

Default:0x20			Register Name: ANA_DAC_CTRL1
Bit	**R/W**	**Default**	**Description**
7:6	R/W	0x0	Reserved
5	R/W	0x1	DAC_OUT_MODE DAC OUTPUT mode control 0: Single mode 1: Differential mode
4	R/W	0x0	Reserved
3	R/W	0x0	DAC_OUT_SEL_DAC DAC OUTPUT source select dac 0: Not select 1: Select
2	R/W	0x0	DAC_OUT_SEL_MIC DAC OUTPUT source select mic input 0: Not select 1: Select
1	R/W	0x0	DAC_OUT_EN DAC OUTPUT STAGE enable 0: Disable 1: Enable
0	R/W	0x0	DAC_DCT_EN DAC DCT enable 0: Disable 1: Enable

Reg_0x81 DAC Analog Control Register 2

Default:0x93			Register Name: ANA_DAC_CTRL2
Bit	**R/W**	**Default**	**Description**
7	R/W	0x1	DAC_AUTO_RAMP

			DAC OUTPUT auto ramp up 0: manual control 1: auto ramp up
6:4	R/W	0x1	DAC_CHARGING_TIME DAC OUTPUT charging time after ramp up 0: 128ms 1: 256ms 2: 384ms 3: 512ms 4: 640ms 5: 768ms 6: 896ms 7: 1024ms
3:1	R/W	0x1	DAC_RAMP_TIME DAC OUTPUT ramp time 0: 256ms 1: 512ms 2: 768ms 3: 1024ms 4: 1280ms 5: 1536ms 6: 1792ms 7: 2048ms
0	R/W	0x1	DAC_RAMP_EN DAC OUTPUT ramp up function enable 0: Disable 1: Enable

Reg_0x83 DAC Analog Control Register 3

Default:0x04			**Register Name: ANA_DAC_CTRL3**
Bit	**R/W**	**Default**	**Description**
7:4	R/W	0x0	Reserved
3:0	R/W	0x4	DAC_OPOUT_OPTIMIZE DAC OPOUT optimize control

Reg_0x84 DAC Analog Tuning Register 1

Default:0x50			**Register Name: ANA_DAC_TUNE1**
Bit	**R/W**	**Default**	**Description**

7:0	R/W	0x50	DAC analog tuning

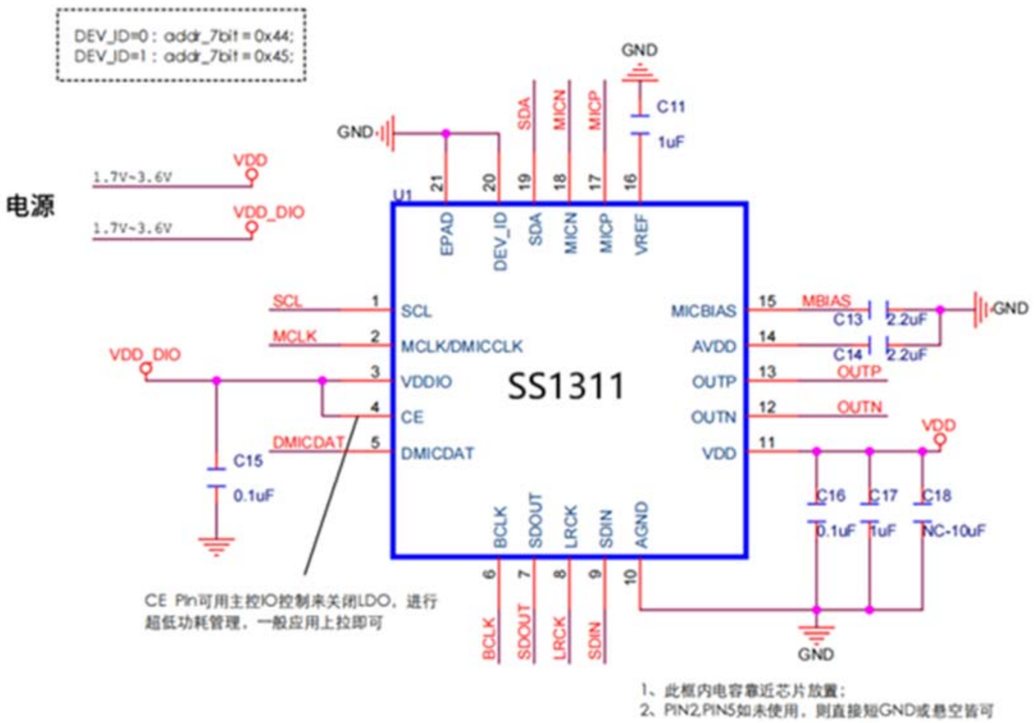
Reg_0x85 DAC Analog Tuning Register 2

Default:0xAA			**Register Name: ANA_DAC_TUNE2**
Bit	**R/W**	**Default**	**Description**
7:0	R/W	0xAA	DAC analog tuning

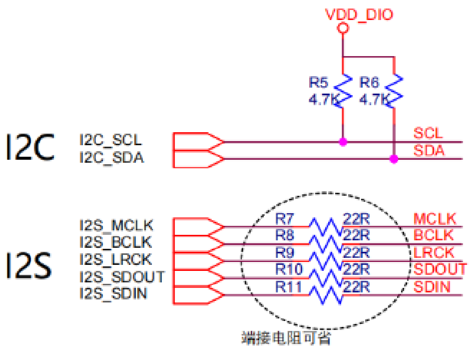
9 SCH

The schematic demo is shown below. Please refer to the evaluation board for a more details.

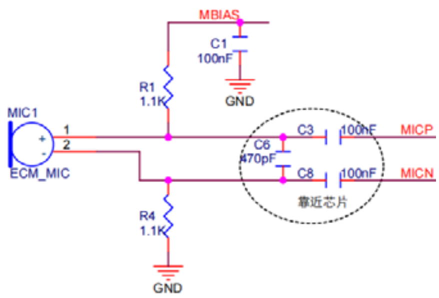
SS1311



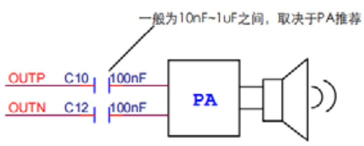
I2C/I2S



ECM_AMIC



SPEAKER

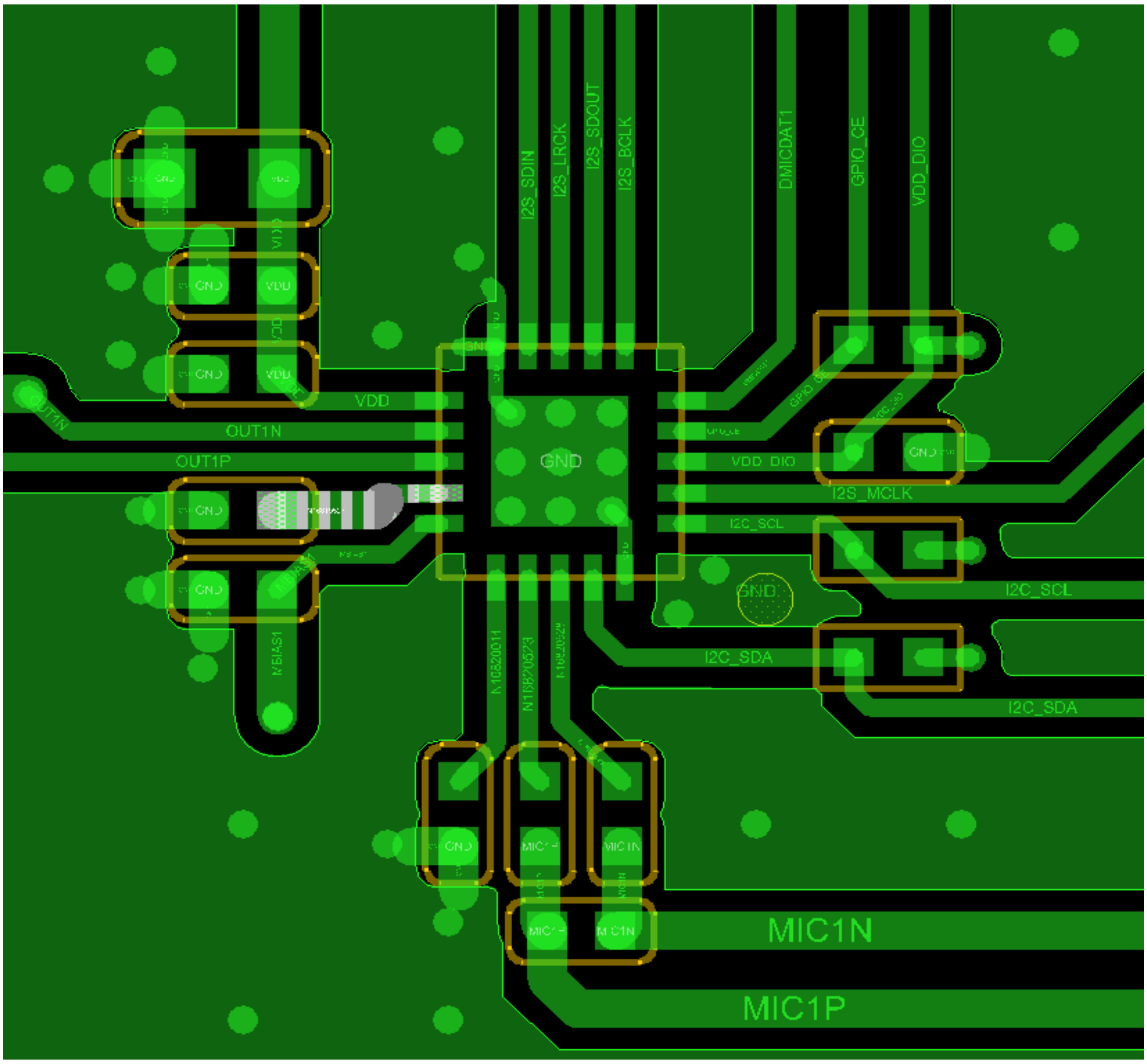


10 PCB

10.1 Layout Guidelines

The following guidelines can optimize the SS1311 performance:

(1) Keep decoupling capacitors as close as possible to SS1311 pins.
(2) Place SS1311 far away from signal radiation source, e.g., RF, DCDC inductor, DRAM, LCD. Use 33pF capacitor close to the input pin to reduce RF interference (optional).
(3) Keep MICP/MICN traces in parallel with GND to the sides if routing through noisy areas such as high speed clocks and high current traces.
(4) Do not route MICP/MICN, OUTP/OUTN signals parallel to other signals over long distances, even if they are on different layers.
(5) The wire from AVDD（Pin-14）to the bypass capacitor should be as wide as possible, and the white-highlighted wire in the example below is 20mil.
(6) Add multiple vias to connect ground planes throughout the board.
(7) When necessary, separate the chip from other devices, e.g., high-power audio PA, high current power supply.



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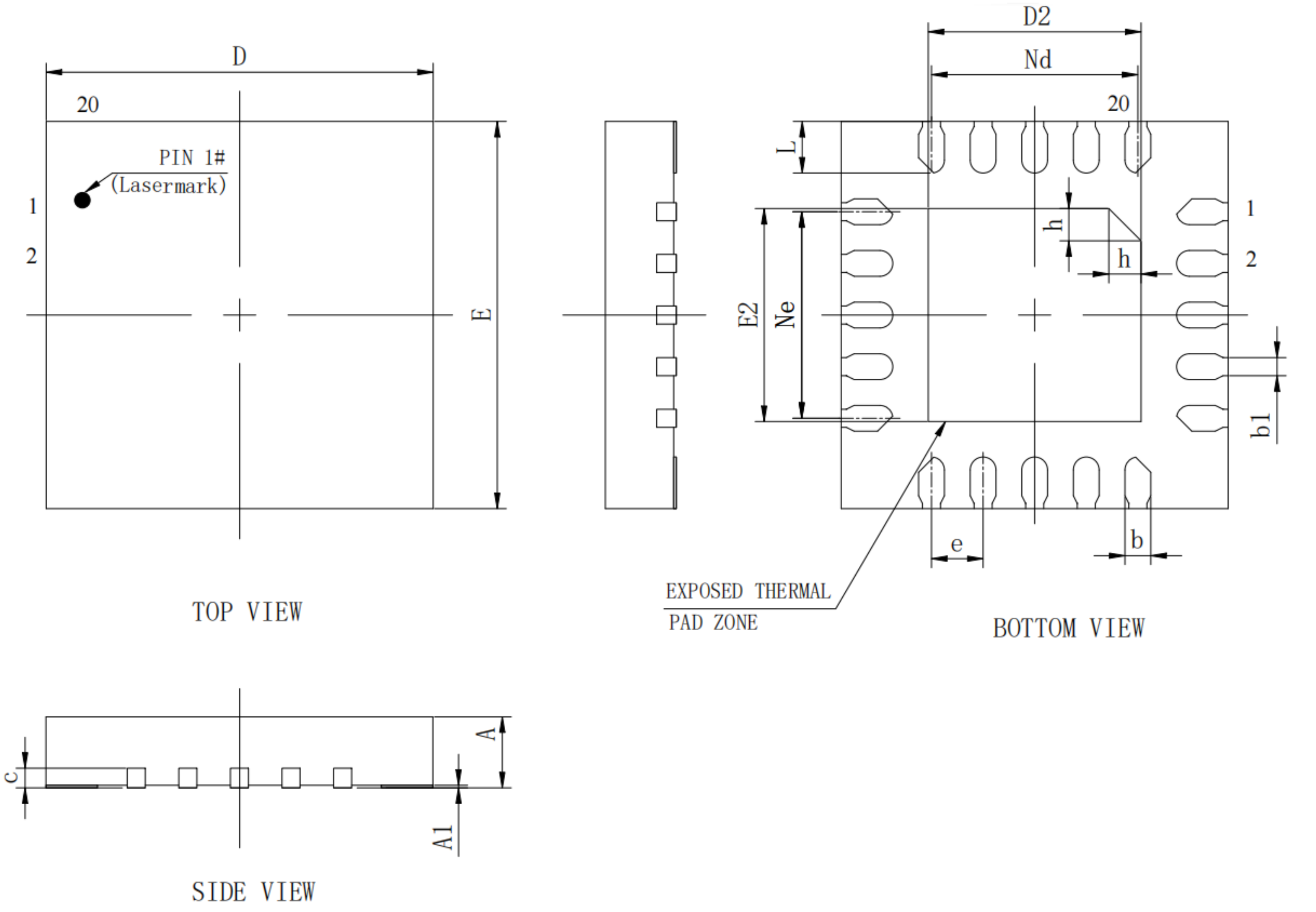
11 Package Outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 50	0.55	0. 60
A1	0	0. 02	0. 05
b	0. 15	0. 20	0. 25
b1	0. 14REF		
c	0. 10	0. 15	0. 20
D	2. 90	3. 00	3. 10
D2	1. 55	1. 65	1. 75
e	0. 40BSC		
Ne	1. 60BSC		
Nd	1. 60BSC		
E	2. 90	3. 00	3. 10
E2	1. 55	1. 65	1. 75
L	0. 35	0. 40	0. 45
h	0. 20	0. 25	0. 30

12 Revision History

REVISION	DATE	DESCRIPTION
1.0	Oct 25, 2024	Initial Release
1.1	Apr 20,2025	Release all

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